UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VIASAT, INC., **Plaintiff,** **vs.** **KIOXIA CORPORATION and KIOXIA AMERICA, INC.,** **Defendants.**	**Case No. 6:21-cv-1231**
VIASAT, INC., **Plaintiff,** **vs.** **WESTERN DIGITAL TECHNOLOGIES, INC.,** **Defendant.**	**Case No. 6:21-cv-1230**

DECLARATION OF DR. STEPHEN B. WICKER REGARDING CLAIM CONSTRUCTION

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I. BACKGROUND

1. My name is Dr. Stephen B. Wicker. I am a Professor of Electrical and Computer Engineering at Cornell University in Ithaca, New York. I have been retained as an expert by counsel for Defendant Western Digital Technologies ("Western Digital") and counsel for Defendants Kioxia Corporation and Kioxia America, Inc. (collectively "Kioxia") in connection with these patent infringement actions filed by Plaintiff Viasat.

2. This report contains statements of my opinions formed to date and the bases and reasons for those opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses, within the guidelines of the Court.

3. I have summarized in this section my educational background, career history, publications, and other relevant qualifications. My full curriculum vitae is attached as Exhibit A to this report.

A. Education

4. I received my Bachelor of Science degree in Electrical Engineering from the University of Virginia in 1982. In 1983, I received a Master of Science degree in Electrical Engineering from Purdue University, and in 1987, I received a Ph.D. in Electrical Engineering from the University of Southern California. My doctoral studies focused on the theory of sequences and error control codes for digital communication systems.

B. Career History

5. From May 1982 to August 1983, I worked for the Network Architecture Research Group of Bell Laboratories, in Columbus, Ohio. While with Bell Laboratories, I worked on digital switching systems for the messages that control the telephone network. From August 1983 through September 1987, I was a System Engineer for the Space and

Communications Group of the Hughes Aircraft Company, in El Segundo, California. While at Hughes Aircraft, I designed and developed wireless communication payloads for commercial, military, and NASA spacecraft. My work at Hughes included acting as the Principal System Engineer for new business in advanced satellite systems.

6. From September 1987 through June 1996, I was a member of the faculty of the School of Electrical and Computer Engineering at Georgia Tech. Since July 1, 1996, I have been a member of the faculty of the School of Electrical and Computer Engineering at Cornell University, where I teach and conduct research in wired and wireless information networks, error control coding, security, and privacy.

7. I have consulted extensively in the telecommunications industry, working with Motorola, Lockheed, Integrated Device Technologies, Unisys, Texas Instruments, and other corporations to develop advanced technologies for their telecommunications products.

8. My current research focuses on wired and wireless communication networks, with an emphasis on security and privacy.

C. Publications and Patents

9. I have written and/or edited six books and roughly two hundred and fifty journal and conference papers, most of which focus on digital communication systems and information networks. My most recent book, entitled *Cellular Convergence and the Death of Privacy*, was published by Oxford University Press in 2013. I am also the author of *Error Control Systems for Digital Communications and Storage* (Prentice Hall, 1995), which has been adopted as a text for courses in over fifty universities in twelve countries. I am the co-author of *Reed-Solomon Codes and their Applications*, published in 1994 by the IEEE Press; *Turbo Coding*, published in November 1998 by

Kluwer Academic Press; and *Fundamentals of Codes, Graphs, and Iterative Decoding*, published in 2002 by Kluwer Academic Press.

10. I have also contributed chapters to several books, including "Privacy-Aware Design for the Monitoring, Control, and Protection of Critical Infrastructure," published in Homeland Security Threats, Countermeasures, and Privacy Issues by Artech House in 2010. A complete list of my publications is contained in my curriculum vitae, a copy of which is appended as Exhibit A to this declaration.

11. I am a named inventor on the following patents.

- Wicker, S.B., "Private Overlay for Information Networks", U.S. Patent No. 9,813,233, 7 November, 2017 – assigned to Cornell University.
- Ober, C.K., O'Rourke, T.D., Spencer, M.G., Turner, J.N., Wicker, S.B., "Flexible Substrate Sensor System For Environmental And Infrastructure Monitoring", U.S. Patent No. 8,701,469, 22 April 2014 – assigned to Cornell University.
- Fontaine, F. and Wicker, S.B., "Method and Apparatus for Turbo Decoding Block Codes", U.S. Patent 7,243,288, 10 July 2007 – assigned to Motorola Inc.
- Wicker, S.B. and Fine, T.L., "Sensor-Assisted ALOHA Multiple Access", U.S. Patent No. 6,404,750, 11 June 2002 – assigned to Cornell University.
- Wang, X.A. and Wicker, S. B., "Artificial Neural Network Viterbi Decoding System and Method," U.S. Patent No. 5,548,684, 20 August, 1996 – assigned to Georgia Tech Research Corporation.

D. Other Relevant Qualifications

12. I have served as an Associate Editor for the *IEEE Transactions on Communications* and the *ACM Transactions on Sensor Networks*. I was twice elected to the Board of Governors of the IEEE Information Theory Society. I have also edited several special issues for a variety of journals and technical magazines, and served a three-year term on the Information Science and Technology Panel for the Defense Advanced Research Projects Agency (DARPA). This panel is responsible for technology assessment for the

U.S. Department of Defense. My DARPA duties included leading a one-year study on wireless sensor networks for defense against biological attack. In 2010, I was appointed to the Air Force Scientific Advisory Board.

13. From 2005 – 2018 I served as the Cornell University Principal Investigator for the TRUST Science and Technology Center – a National Science Foundation center dedicated to the development of technologies for securing the nation's critical infrastructure. In 2011, I was named a Fellow of the IEEE for contributions to wireless information systems.

14. In 2014 I briefed the staff of the National Economic Council at the White House on the subject of privacy-aware designs for cellular networks and the smart grid.

15. I have taught error control coding in particular, and digital systems in general to thousands of students at Georgia Tech and Cornell over the past thirty-five years. I have been the recipient of four Cornell University College of Engineering faculty teaching awards.

E. Materials and Other Information Considered

16. I have considered information from various sources in forming my opinions, including the Asserted Patents, their prosecution histories, and all the documents referenced in this declaration. I have also drawn on four decades of research and development in the area of error control coding and communication networks.

F. Prior Testimony

17. The cases in which I have testified as an expert at trial or by deposition within the preceding five years are as follows:

- AMO Development v. Alcon Vision, LLC (for the defendant)
- Sonrai v. Samsung et al. (for the respondents)
- IPCom v AT&T et al (for the defendants)

- Barkan v. Nokia and TMobile (for the defendants)
- Teradyne v. Astronics (for the defendant)
- Huawei v. Verizon (for the defendant)
- Google v. Sonos (for the defendant)
- Barkan v. Sprint (for the defendant)
- Gigamon v. Apcon (for the defendant)
- Impact Engine v. Google (for the plaintiff)
- Sprint v. Altice et al. (for the plaintiff)
- SEVEN Networks v. Apple (for the defendant)
- KAIFI v. AT&T (for the defendant)
- Sprint v. Charter et al. (for the plaintiff)
- INVT v. Apple et al. (for the defendants)
- Intellectual Ventures v. Ericsson and TMobile (for the defendants)
- KPN v. Sierra Wireless (for the defendant)
- Live Person v. 24/7 (for the plaintiff)
- Apple v. Qualcomm (for the plaintiff)
- Motorola v. Hytera (for the plaintiff)
- IP Bridge v TCL (for the defendant)
- Elbit v. Hughes (for the defendant)
- Viatech v. Microsoft (for the defendant)
- Intellectual Ventures v. AT&T, Sprint, and T-Mobile (for the defendants)
- Sprint v. Cox Cable (for the plaintiff)
- PMC v. Apple (for the defendant)

G. Compensation

18. For time spent in connection with study and analysis in this matter, I will be compensated in the amount of $850 per hour. For time spent in connection with testifying in this matter, I will be compensated in the amount of $850 per hour. My compensation does not depend on the outcome of this case.

II. SUMMARY OF OPINIONS

19. I have been asked by Western Digital to provide my expert testimony and opinions regarding certain terms and phrases in U.S. Patent Nos. 8,615,700 (the ‘700 patent) and 8,966,347 (the ‘347 patent) (collectively, “Asserted Patents” or “asserted patents”). The Asserted Patents are directed to error control coding for flash memory.

20. This declaration provides my opinions to date regarding certain claim terms and phrases in the Asserted Patents, although I may provide further testimony and opinions if asked to testify in court or in a deposition. I also reserve the right to supplement or amend my opinions, as well as the bases for those opinions, if I receive additional relevant information or to respond to opinions offered by other experts in this case. I may rely on demonstrative exhibits, including pictures, figures, and drawings that appear in this declaration and the referenced materials.

III. UNDERSTANDING OF THE LAW

21. I am not an attorney. My understanding of the relevant legal principles is based on information provided to me by counsel. I have applied the following legal principles provided to me by counsel in arriving at the opinions set forth herein.

A. Claim Construction

22. I understand that a claim term or phrase is construed according to its ordinary and accustomed meaning as understood by a person of ordinary skill in the art ("POSITA") in the context of the patent at the time of the invention.

23. I understand that patent claims are to be construed in light of the intrinsic record of the patent, which includes the words of the claims; the specification (including the drawings) of the patent; and the prosecution history of the patent, including the cited references. This type of evidence is referred to as "intrinsic" evidence.

24. I understand that the context of any disputed term within the claim language itself is of primary importance. Additionally, I understand that a POSITA is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.

25. I understand that, in addition to the claims and specification, the prosecution history should also be considered. It is my understanding that the prosecution history provides evidence of how the patentee and the examiner viewed the patent, and that the public has a right to rely on the patent applicant's remarks made during prosecution in determining the scope of the claimed invention. Where the specification describes a claim term broadly, arguments and amendments made during prosecution may require a narrower interpretation. For example, I understand that an applicant may disclaim claim scope by amending claims in response to a rejection, or making specific arguments distinguishing the claimed invention over cited prior art.

26. I have been informed that the Court may consider additional evidence, in certain circumstances, which is outside the patent and prosecution history. This type of evidence is known as "extrinsic" evidence. Extrinsic evidence can include expert opinion (including opinions regarding what a POSITA would have known or understood and what a POSITA would not be able to ascertain), dictionaries, treatises, and testimony. However, while extrinsic evidence can shed useful light on the relevant art, I understand that it is less significant than the intrinsic record in determining the legally operative meaning of claim language. Extrinsic evidence can be useful to, for example, provide background on the technology at issue, explain how an invention works, ensure that the Court's understanding of the technical aspects of the patent is consistent with that of a POSITA, or establish that a particular term in the patent or the prior art has a particular meaning in the pertinent field.

27. I understand that in certain instances a patentee may act as its own lexicographer so as to set forth a definition of a claim term other than its plain and ordinary meaning.

However, I further understand that to do so it is not enough for a patentee to simply disclose a single embodiment or use a word in the same manner in all embodiments, the patentee must "clearly express an intent" to redefine the term.

28. I understand that claim elements may be expressed as a means for performing a specified function, and that these are referred to as "means-plus-function" elements.

29. I further understand that claim terms reciting "means for" performing a certain function are presumptively interpreted as means-plus-function terms, and terms omitting this phrase are presumptively not interpreted as means-plus-function terms.

30. However, I further understand that when a claim term lacks the "means for" phrase the presumption can be overcome and means-plus-function interpretation will govern if the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function.

31. I understand that construing a means-plus-function term is a two-step process. First, one must identify the claimed function or functions of the term. Second, one must identify the corresponding structure in the specification, if any, that performs each function.

32. I further understand that, for the specification to disclose corresponding structure, the specification or prosecution must clearly link or associate that structure to the function recited in the claim. I also understand that, even if the specification discloses corresponding structure, the disclosure must be of adequate corresponding structure to achieve the claimed function. The specification must disclose the structure such that a POSITA can recognize the structure in the specification and associate it with the corresponding function in the claim, otherwise the claim is indefinite (addressed below

in Section VII). I understand that it is insufficient merely for a POSITA to have been able to devise or otherwise implement a structure to perform the claimed function.

33. I understand that if a function recited by a means-plus-function limitation is computer-implemented—and a general-purpose computer cannot perform the function without special programming (software)—the specification must disclose the structure in the form of an algorithm. I understand that an algorithm is a step-by-step procedure for performing the claimed function. I understand that such an algorithm can be expressed in many forms, including flow charts, a series of specific steps, mathematical formula, prose, and so on. I understand that a restatement of the function itself in the specification is inadequate to disclose an algorithm for performing the claimed function.

34. I understand that the same algorithmic requirement and analysis applies if a function recited by a means-plus-function limitation is implemented by a process or in computer-readable media or storage devices (such as flash memory).

B. Indefiniteness

35. I understand that a patent must include one or more claims that particularly point out and distinctly claim the subject matter regarded as the invention. I understand that a claim is indefinite, and therefore invalid, if it fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention when viewed in light of the intrinsic evidence.

36. I understand that when a term of degree is used in a claim, the patent must provide some standard for measuring that degree. Likewise, when a subjective term is used in a claim, the patent must provide some standard for measuring the scope of the term. The standard must provide objective boundaries for those of skill in the art.

37. I understand that a means-plus-function claim is indefinite if a POSITA would be unable to recognize the structure in the specification and associate it with the corresponding function in the claim. For example, in the context of a computer-implemented (or implemented by a process or computer readable media or storage device) means-plus-function limitation that requires special programming, the claim is indefinite if the specification fails to disclose an algorithm for performing the claimed function. I understand that, if a claim recites multiple functions, the specification must recite an algorithm for performing each function. I also understand that, to disclose an algorithm, the specification must do more than merely restate the function recited in the claim. The specification cannot simply disclose a black box that performs the recited function. Instead, I understand that the specification must disclose a specific algorithm for performing the claimed functions. I further understand that general reference to an algorithm or class of algorithms that place no limitations on how values are calculated, combined, or weighted is insufficient to make the bounds of the claim understandable.

38. I understand that simply disclosing software without providing some detail about the means to accomplish the function is not enough. I understand that—even if the specification does disclose an algorithm—it must disclose an algorithm that, from the viewpoint of a POSITA, is sufficient to define the structure and make the bounds of the claim understandable. I understand that the specification itself must disclose the requisite structure to a POSITA, including—in the context of a computer-implemented means-plus-function limitation—a sufficient algorithm. I understand that a specification does not disclose requisite structure if a POSITA must choose an appropriate algorithm and process it into a microprocessor or design or otherwise devise the requisite structure

in view of the specification. I understand that a description of an algorithm that places no limitations on how values are calculated, combined, or weighted is insufficient to make the bounds of the claim understandable. Additionally, an algorithm that does not identify all of the operations necessary to perform a claimed function and fails to provide the arguments each operation may require does not disclose sufficient defining structure.

IV. LEVEL OF ORDINARY SKILL IN THE ART

39. I understand that the relevant time period of the invention is August 18, 2010, the filing date of the non-provisional application leading to the asserted patents. My opinions would not change if the relevant time period of the invention were August 18, 2009, the filing date of the provisional application to which the asserted patents claim priority.

40. Based upon my education and experience, I am very familiar with the level of relevant knowledge about the technology at issue that one of ordinary skill in the art would have possessed during the relevant timeframe. As a faculty member at Georgia Tech and then Cornell University, I have conducted research, written and presented papers, published books, and taught classes on error control during this timeframe, and I am very familiar with the state of the art in the technological field of the Asserted Patents at that time.

41. In determining the characteristics of a hypothetical person of ordinary skill in the art of the Asserted Patents in the relevant timeframes, I considered several things, including the various approaches to telecommunications systems and wireless location employed in the prior art, the type of problems encountered, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field. Finally, I placed myself back in the relevant timeframe and considered the engineers

that I had taught and worked with. I came to the conclusion that a person of ordinary skill in the field of art of the Asserted Patents would be a person with a B.S. in electrical engineering or computer science or a related degree, and four years' experience designing, developing, or researching error correction coding systems. Additional education might compensate for less experience, and vice-versa. My opinions do not depend on this precise definition and would be the same from the perspective of any reasonable POSITA.

V. BACKGROUND TECHNOLOGY

42. Error control coding (also called channel coding) is the addition of redundancy—or additional bits derived from the original information—to an information stream so that the receiver can detect and/or correct errors in received data. Error control has been recognized as an important element in digital communications since the late 1940s. It has been well understood for over fifty years that error control codes are a powerful means for improving the performance of a digital communication channel.

43. Error control coding also directly affects the data rate and capacity of a system. While error control coding improves performance of the communication system in various ways, it also uses some of the capacity of the system to transmit redundant information. As a result, the system cannot be as efficient as its actual capacity.

44. The efficiency of an error control code is typically defined as the "coding rate." For example, if a particular code has a coding rate of 3/5, that means for every 5 bits transmitted, only 3 are non-redundant information bits, typically called parity data.

45. Not all error control codes are created equal, however. Different error control codes may be more or less effective at detecting and/or correcting errors for a given coding

rate. Thus, a very effective error control code may be able to provide the same BER at rate ¾ as a less effective error control code would provide at rate ½. Thus, creating and using new, better error control codes allows communications system providers to realize the benefits of error control while still maximizing the capacity of the system.

46. The simplest form of error control is repetition; for example, if a transmitter repeats every bit of information three times, the presence of errors in the received data is easier to detect. In the simple example below, we can see that one of the received bits (underlined) is in error.

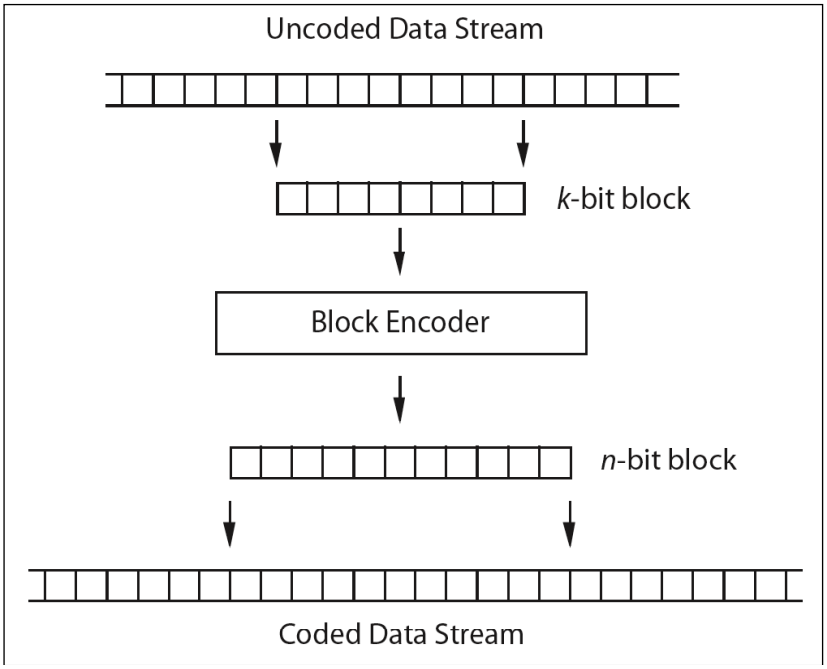
Data:	0, 1, 0, 0, 1
Transmitted:	000, 111, 000, 000, 111
Received:	000, 111, 000, 100, 111

47. In this particular example, we can actually correct a single error. As every information bit is repeated three times by the transmitter, the receiver can correct errors by taking three received bits at a time and determining the majority value within the set. In the case of the received 100, the majority value is a zero - we correct the erroneous one by using the other bits to determine what was most likely to have been sent.

48. Simple repetition is an inefficient form of error control. There are many other schemes that perform much better (and are also much more complicated). Such codes include the Reed-Muller, LDPC, and turbo codes used in, *e.g.*, cellular technology.

49. The first error control codes developed were block codes. A block code is a set of codewords of fixed length. Encoding with block codes takes the form of a fixed mapping from k-bit blocks of information onto n-bit codewords. As the codeword

length n is greater than the information block length k, redundancy is introduced that can be used to detect and/or correct errors. Examples of block codes include Hamming, Reed-Muller, Reed-Solomon, BCH, and Golay codes.



50. As seen above, block codes add redundant bits to the data. This allows the receiver to correct and/or detect errors that occur during transmission. The concept of adding redundant bits dates back at least to the late 1940s, when Shannon described Hamming Codes in his "Mathematical Theory of Communication." In general, the algorithms by which this is done depend on the specific code, system requirements, and available resources; see, for example, *Error Control Systems for Digital Communication and Storage* by S. B. Wicker.

51. In the mid 1950s convolutional coding was developed as another means for adding redundant bits to a data stream. A convolutional encoder converts the entire data stream, regardless of its length, into a single coded stream.

52. Convolutional codes were first presented by Elias in 1955.[1] He showed that redundancy can be introduced into a data stream through the use of a linear shift register that performs simple mathematical addition on the bits as they are fed through the encoder.

A. Error Correction vs. Error Detection

53. Error detection is defined as the determination of whether or not errors are present in a received word, where the word is the received (possibly corrupted) version of the transmitted codeword.

> *The determination of whether errors are present in a received word is error detection .*
>
> [Chapter 4, *Error Control Systems for Digital Communication and Storage*, Wicker 1995]

54. The "received word" shown below consists of the transmitted codeword plus an error pattern **e**. Error detection consists of determining whether or not **e** is all-zeros (no errors) or has one or more nonzero values (errors are present).

[1] P. Elias, "Coding for Noisy Channels," *IRE Conv. Record*, Part 4, pp. 37 - 47, 1955.

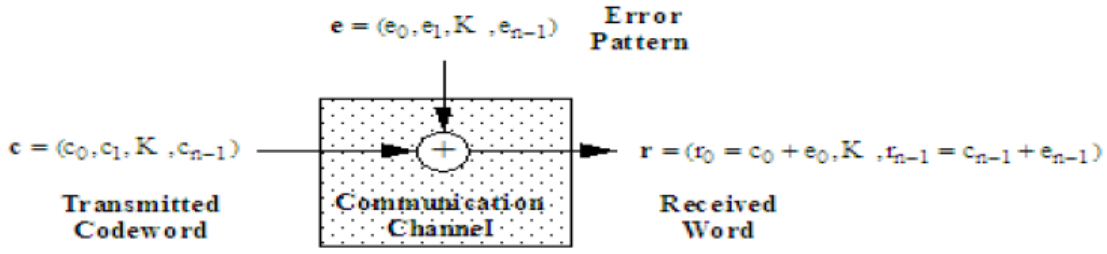


Figure 4.2: Baseband model for an additive noisy channel

55. Error correction (often referred to as forward error correction, or FEC) does not focus on detecting errors, but instead attempts to map what is received to a valid codeword or directly to the original information.

In FEC [Forward Error Correcting] systems the arithmetic or algebraic structure of the code is used to determine which of the valid code words is most likely to have been sent given the erroneous received word.

[Chapter 4, *Error Control Systems for Digital Communication and Storage*, Wicker 1995]

56. Convolutional, turbo and LDPC decoders perform error correction through the use of "soft decision decoding." Soft decision decoders operate on soft inputs, *i.e.*, quantized versions of the received waveforms meant to capture the level of uncertainty in the values of the bits within any given received word. As described below, they DO NOT operate on hard inputs, *i.e.*, the zeros and ones used in error detection schemes.

In soft decision decoding the receiver takes advantage of "side information" generated by the receiver bit decision circuitry. Rather than simply assign a zero or a one to each received, noisy binary signal, a more flexible approach is taken through the use of multi-bit quantization. Four or more decision regions are established, ranging from a "strong one" decision to a "strong zero" decision. Intermediate values are given to signals for which the decision is less clear.

[Chapter 12, *Error Control Systems for Digital Communication and Storage*, Wicker 1995; emphasis added]

57. More specifically, the Viterbi based decoders that are commonly used for the decoding of convolutional codes performs sequence estimation on quantized received waveforms, providing the maximum likelihood estimate of the transmitted codewords given what was received. Turbo and LDPC decoders perform sequence estimation on quantized received waveforms, providing an estimate of the *original data* given what was received. In neither case does the decoder ever look at post-memory cell read zeros and ones and determine whether or not errors have occurred.

B. BCH Codes

58. BCH and Reed-Solomon codes form the core of the most powerful known algebraic codes and have seen widespread application in the past sixty years[2]. The fundamental work on BCH codes was conducted by two independent research teams that published their results at roughly the same time. Binary BCH codes were discussed as a generalization of Hamming's work by A. Hocquenghem in a 1959 paper entitled "Codes correcteur d'erreurs.[3]" This was followed in March and September of 1960 by Bose and Ray-Chaudhuri's publications on "Error Correcting Binary Group Codes.[4]" Given their simultaneous discovery of these codes, all three gentlemen have given their name to what are now called BCH codes.

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[2] See Chapter 8, S. B. Wicker, *Error Control Systems for Digital Communication and Storage*,1995.
[3] A. Hocquenghem, "Codes Correcteurs d'Erreurs," Chiffres, Vol. 2, pp. 147-156, 1959.
[4] See R. C. Bose and D. K. Ray-Chaudhuri, "On a Class of Error Correcting Binary Group Codes," *Information and Control*, Vol. 3, pp. 68-79, March 1960 and R. C. Bose and D. K. Ray-Chaudhuri, "Further Results on Error Correcting Binary Group Codes," *Information and Control*, Vol. 3, pp. 279-290, September 1960.

Binary BCH codes are "polynomial codes" that have seen prominent use in satellite communications, paging, and other communication systems since 1960.

C. Turbo Error Control

59. On May 25, 1993, Berrou, Glavieux, and Thitimajshima presented a paper entitled "Near Shannon-Limit Error Correction Coding: Turbo Codes"[5] at the 1993 International Conference on Communications in Geneva. In their paper, Berrou *et al*. described a new class of codes—"turbo codes"— that, along with a new class of suboptimal decoding algorithms, provided error control performance that was only a few tenths of a dB from the Shannon limit (the theoretical rate at which information can be reliably transferred). These turbo codes offered the best solution to date for the problem of power-limited communication on an AWGN channel.[6]

60. Turbo error control is a type of error control that adds redundant information to an encoded message that is later used to estimate the original information sequence. It follows that that turbo error control does not perform error detection.

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[5] C. Berrou. A. Glavieux and P. Thitimajshima. Near Shannon limit error-correcting coding and decoding:
Turbo codes. *Proc. of the 1993 IEEE Internal. Communications Conf*., Geneva, Switzerland (May 23- 26.
1993). 1064-1070.

[6] See, for example, D. Divsalar and F. Pollara. Multiple Turbo codes for deep-space communication, TDA Progress Report 42-121. JPL (May 1995) and S. Dolinar and D. Divsalar, Weight distributions for Turbo codes using random and nonrandom permutations.TDA, Progress Report 42-121. JPL (August 1995).

D. LDPC Codes

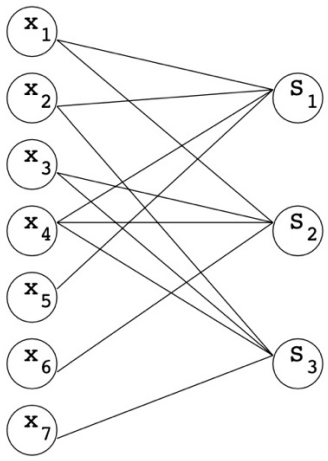
61. Robert Gallager introduced low-density parity-check codes in his doctoral thesis in 1961. Low-density parity-check codes are a special class of linear codes in which the parity check matrices are sparse or of low density (*i.e.*, they consist mostly of zeros).[7] Associated decoding schemes are of much more recent vintage, growing out of the message-passing algorithms developed in the 1990's.

62. LDPC encoding is based on a relatively simple principle. Parity check codes are defined as codes in which selected sets of bits in the codeword must sum to 0 mod 2. The structure of these codes flows in a straightforward way from the mathematics of vector spaces. An example of a parity-check code is the (7,4)-Hamming code for which the following is a valid parity-check matrix **H**.

$$H = \begin{pmatrix} 1 & 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 1 \end{pmatrix}$$

63. A binary vector **c** is a valid codeword for the above hamming code if $\mathbf{cH}^T = \mathbf{0}$. It follows that if $\{x_1, x_2, x_3, x_4\}$ is the set of information bits, then $\{x_5, x_6, x_7\}$ is the set of parity bits where $x_5 = x_1 \oplus x_2 \oplus x_4$, $x_6 = x_1 \oplus x_3 \oplus x_4$, and $x_7 = x_2 \oplus x_3 \oplus x_4$, where $\oplus$ represents addition modulo 2. The parity expressions may be represented in the form of a graph (as seen below), in which the vertices on the right are associated with subsets of the bits on the left that must sum to zero.

[7] See chapter 8 of S. B. Wicker and Kim, S., *Fundamentals of Codes, Graphs, and Iterative Decoding*, Boston: Kluwer Academic Press, 2002.



64. Using this graph representation, it is possible to apply the above-mentioned message-passing algorithms to decode received words and obtain excellent error control performance. *See* S. B. Wicker and Kim, S., *Fundamentals of Codes, Graphs, and Iterative Decoding*, Boston: Kluwer Academic Press, 2002.

E. Final Comments on Error Control Codes

65. It has been my experience over the past forty plus years that there were dozens of texts on the subject of error control, and thousands of related journal and conference papers available at the prioity dates of the patents at suit. I note the following texts (a very partial list) that include at least some of the above types of error control.

- J. Viterbi and J. K. Omura, *Principles of Digital Communication and Coding*, New York: McGraw Hill, 1979 (block and convolutional coding).
- R. E. Blahut, *Theory and Practice of Error Control Codes*, Reading: Addison-Wesley, 1983 (block and convolutional coding).
- M. Michelson and A. H. Levesque, *Error Control Techniques for Digital Communication*, New York: Wiley, 1985 (block and convolutional coding).
- S. A. Vanstone and P. C. van Oorschot, An Introduction to Error Correcting Codes with Applications, Boston: Kluwer, 1989 (block coding).
- Biglieri, et al., Introduction to Trellis-Coded Modulation with Applications (Macmillan Publishing Co. 1991) (TCM coding).
- Wicker, S. B. and Bhargava, V. K. (editors), *Reed-Solomon Codes and Their Applications*, Piscataway: IEEE Press, 1994 (block coding).

- Wicker, S. B., *Error Control Systems for Digital Communication and Storage*, Englewood Cliffs: Prentice Hall, 1995 (block, convolutional and TCM coding).
- Wicker, S. B. and Kim, S., *Fundamentals of Codes, Graphs, and Iterative Decoding*, Boston: Kluwer Academic Press, 2002 (LDPC and Turbo Coding).
- Heegard, C. and Wicker, S. B., *Turbo Coding*, Boston: Kluwer Academic Press, 1999 (Turbo Coding).
- Wicker, S. B. and Bhargava, V. K. (editors), *Reed-Solomon Codes and Their Applications*, Piscataway: IEEE Press, 1994 (BCH and Reed-Solomon Codes).

VI. OVERVIEW OF THE ASSERTED PATENTS

66. The ’700 patent and ’347 patent share a common specification. Though I cite to only the ’700 patent in this section, the same disclosure is found in the ’347 patent.

67. The asserted patents state that it “relates to forward error correction (FEC) in general and, in particular, to FEC for flash memory.” ’700 patent, 1:16-17.

68. The patents further state by way of background:

> The advancements of flash memory technology in recent years has dramatically increased storage capacity and decreased the cost of non-volatile semiconductor memory. This has made Solid State Drives (SSDs) (typically a flash memory-based non-volatile memory system) an emerging substitute for magnetic Hard Disk Drive (HDD).

’700 patent, 1:18-23.

69. The patents further allege that “use of FEC to enhance the reliability and longevity of flash memory is one of the challenges for making SSDs perform on par with HDDs.” ’700 patent, 1:24-26.

70. In the “Detailed Description” sections, the patents state that “[s]ystems, devices, methods, and software are described for FEC for flash memory.” ’700 patent, 3:23-24.

71. According to the patents:

> Because of this increase in density and the related issues in manufacturing, one of the challenges for flash memory is to maintain high reliability and longevity. The deterioration of the oxide over time, and the disruptions from neighboring memory pages, can lead to data retention and corruption issues translating into bit errors. While the chances of any given data bit being corrupted is quite small, the vast number of data bits in a storage system makes the likelihood of data corruption a very real possibility. FEC may be one of the tools used to address these bit errors to improve the reliability and lifespan of flash memory.

'700 patent, 3:12-22.

72. Figure 1 of the patents, reproduced below, "is a block diagram of a flash memory decoder system according to various embodiments of the invention." '700 patent, 2:4-5.

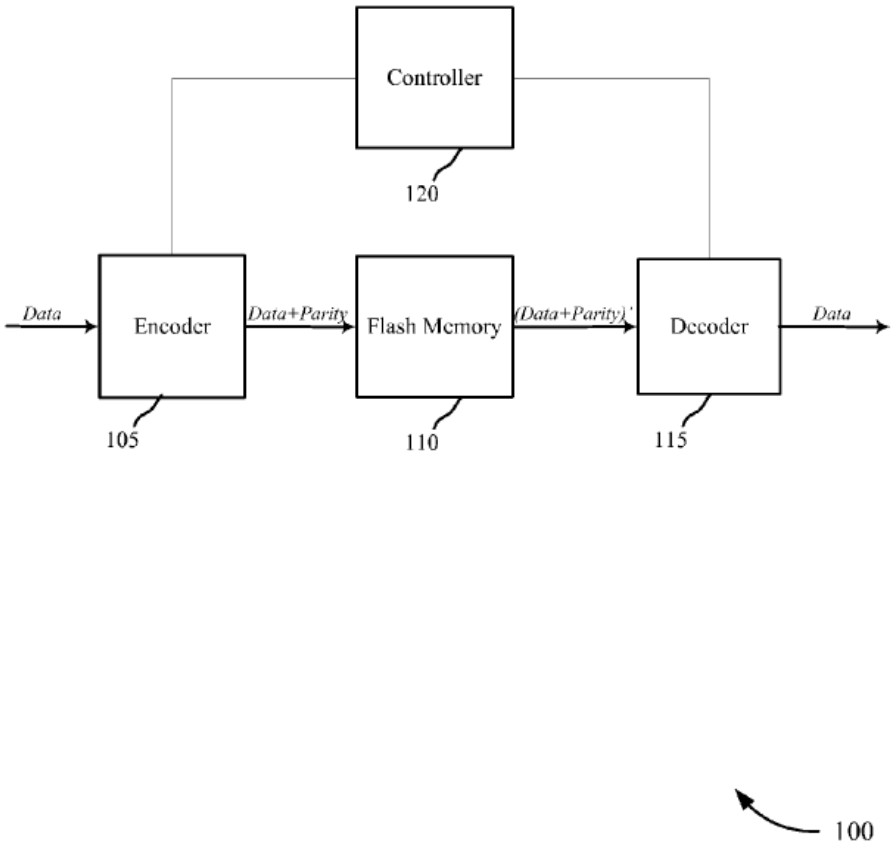


FIG. 1

73. Per the patents, Figure 1 shows "a flash memory system 100" which "includes an encoder 105, flash memory 110, a decoder 115, and a controller 120." '700 patent, 3:24-26. The patents note that the "flash memory system 100 may be a stand-alone device, or may be integrated (in whole or in part) with a computer, server, phone or mobile device, tablet, television, or any other computing device." '700 patent, 3:27-30.

74. The patents also state that:

> Each of these system 100 components may be in communication with each other. The encoder 105, decoder 115, and controller 120 may, individually

> or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

'700 patent, 3:31-45.

75. The patents explain that "encoder 105 may receive data to be stored, and encode the data (e.g., adding parity information) for storage in the flash memory 110 as encoded data." '700 patent, 3:46-48.

76. In Figure 2, reproduced below, the patents disclose "a block diagram of a flash memory decoder according to various embodiments of the invention." '700 patent, 2:7-8.

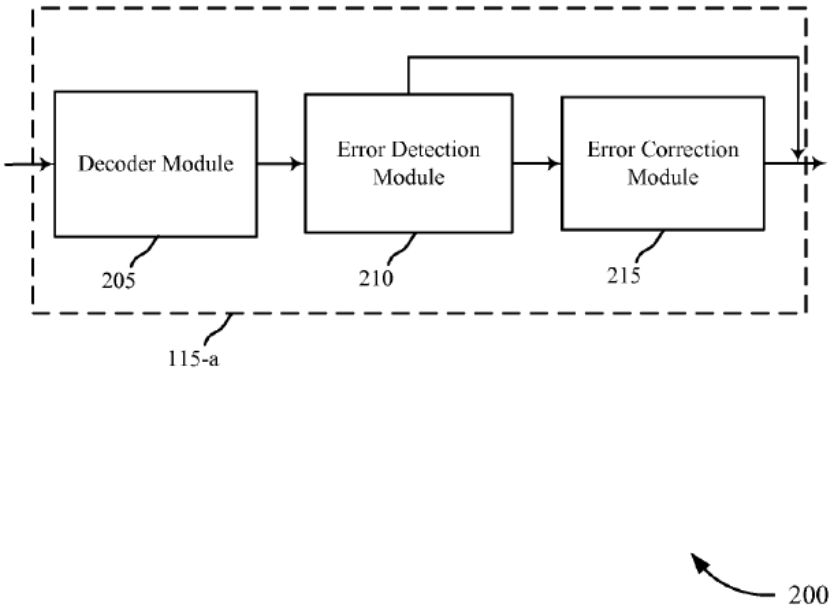


FIG. 2

77. The patents further describe Figure 2 as follows:

> FIG. 2 is a block diagram 200 of a flash memory decoder 115-*a* according to various embodiments of the invention. The flash memory decoder 115-*a* may, for example, be the decoder 115 of FIG. 1, although flash memory decoder 115-*a* may be implemented in a number of other systems and devices, as well. The flash memory decoder 115-*a* includes a decoder module 205, an error detection module 210, and an error correction module 215, and each of may be in communication with each other. In one example, the error detection module 210 includes a number of sub-modules configured to detect errors on decoded streams of data. The error correction module 215 may be physically separate from each error detection sub-

> module, and may also include a number of sub-modules (each of which may be time-shared by a number of error detection sub-modules.
>
> These components and sub-modules therein may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

'700 patent, 5:47-6:8.

78. The patents further state that:

> The decoder module 205 may receive encoded data from flash memory, and … generate decoded (or partially decoded) data streams. As noted, the error detection module 210 may include a number of error detection sub-modules operating in parallel. Each (or a subset) of the error detection sub-modules may receive a different one of the data streams, and evaluate the respective stream to determine whether a portion of the stream contains an error. Each error detection sub-module may forward the portion of the respective

> received stream containing an error to the error correction module 215 (bypassing the error correction module 215 with the error-free portions). The error correction module 215 corrects the received portions of the respective received streams containing an error. As noted above, the error correction module 215 may include a number of sub-modules (each of which may be time-shared by a number of error detection sub-modules).

'700 patent, 6:9-28.

79. Figure 3 in the patents, reproduced below, depicts "a block diagram illustrating an example of an architecture for a flash memory decoder system 300 more particularly illustrating error detection and correction sub-modules" and states that this configuration is an example of the system 100 of FIG. 1. '700 patent, 6:29-33.

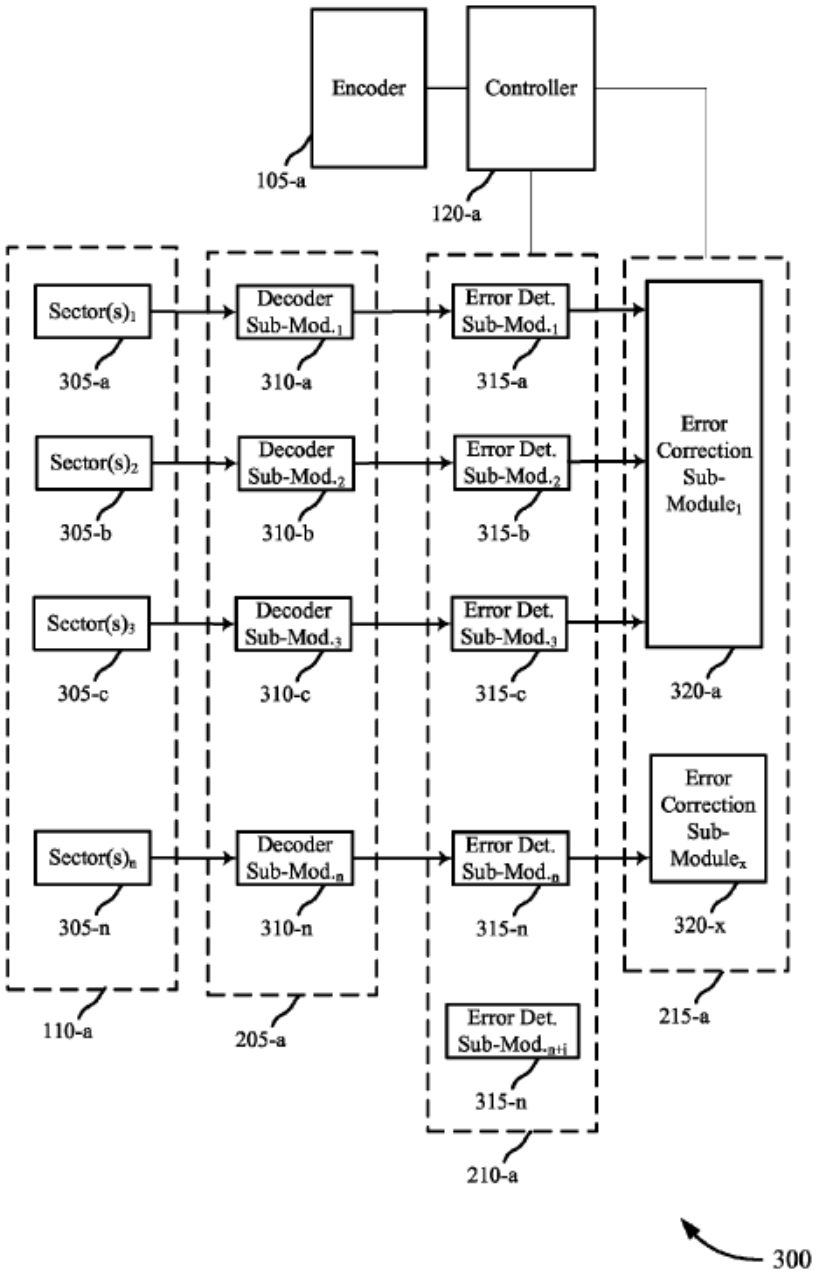


FIG. 3

80. With further reference to Figure 3, the patents state:

The flash memory 110-*a* includes a number of different sets of one or more active sectors 305. The decoder module 205-*a* includes a number of decoder

sub-modules 310, and each decoder sub-module 310 may be associated with a different set of sectors 305. The error detection module 210-*a* includes a number of error detection sub-modules 315, and each decoder sub-module 310 may be associated with a different set of sectors 305. Thus, encoded data may be read from a set of one or more of sectors 305 (e.g., sector(s) 305-*a*) by a decoder sub-module 310 (e.g., decoder sub-module 310-*a*), and processed (e.g., buffered, de-interleaved, decoded to some extent, etc.) to generate a data stream. The data stream may be forwarded to an error detection sub-module 315 (error detection sub-module 315-*a*). Thus, encoded data from a set of one or more of sectors 305-*a* may be sent to an error detection sub-module 315-*a*. Different sets of sectors 305 may each send their respective data via different decoder sub-modules 310, as illustrated. In one embodiment, each error detection sub-module 315 is distinct from each other. In other embodiments, the decoder sub-module 310 and error detection sub-module 315 may be integrated to varying degrees.

Each error detection sub-module 315 may evaluate the respective stream to determine whether a portion of the stream contains an error. Each error detection sub-module 315 may forward the portion of the respective received stream containing an error to the error correction module 215-*a* (bypassing the error correction module 215 with the error-free portions). The error correction module 215-*a* includes a number of error correction sub-modules 320, each error correction sub-module 320 responsible for handling the errors from a number of error detection sub-modules 315 (e.g., error correction sub-

> module 320 may correct errors from error detection sub-modules 315-*a*, -*b*, and -*c*). Error correction sub-modules 320 may correct the received portions of the respective received streams containing an error. Each error correction sub-module 320 may receive portions of streams with errors, and these portion may have been detected in parallel.
>
> Controller 120-*a* may perform a number of functions in the decoder process. Controller 120-*a* may dynamically modify the error detection sub-modules 315 and the error correction sub-modules 320 assigned to sectors 305 of flash memory 110-*a*. The controller 120-*a* may selectively power-up one or more of the error correction sub-modules 320 responsive to a monitored age or error rate associated with the flash memory 110-*a*. The controller 120-*a* may perform this monitoring on a per-sector basis, and the error correction sub-modules 320 may be powered-up to serve the sectors 305 where the error rates exceed a threshold. The controller 120-*a* may adapt the coding rate to be used by the encoder responsive to a monitored age or error rate associated with the flash memory 110-*a*. The controller 120-*a* may perform this monitoring on a per-sector basis, and the controller 120-*a* may adapt the coding rate on a per sector basis.

’700 patent, 6:39-7:26.

81. Figure 4 (below) depicts another “example of the system 100 of FIG. 1.” ‘’700 patent, 7:31-34.

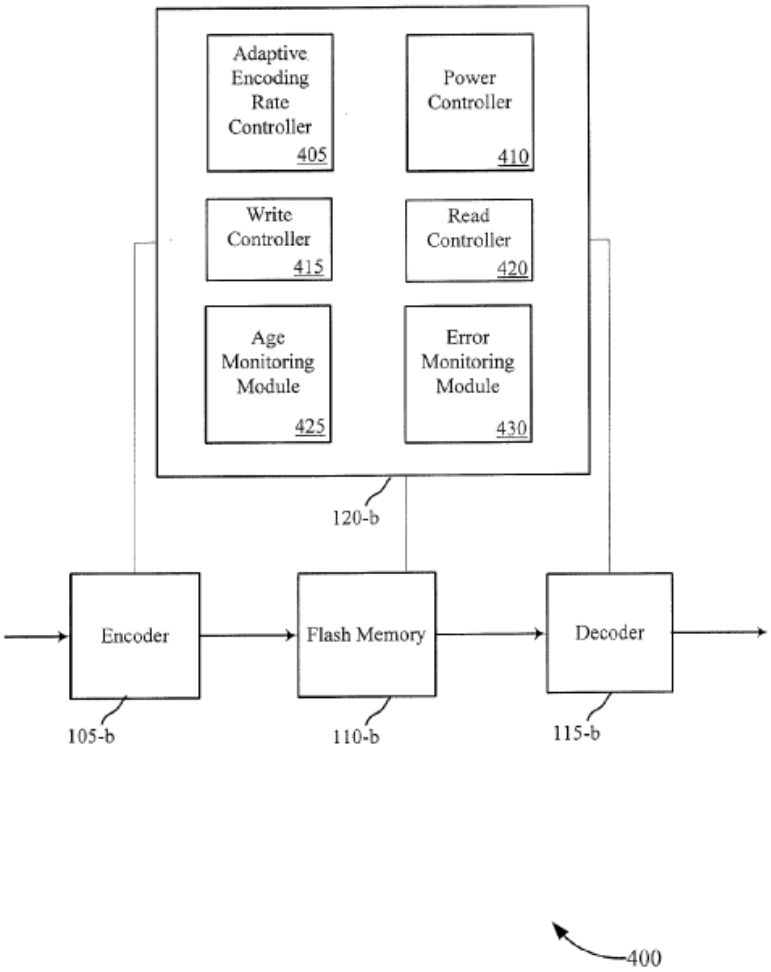


FIG. 4

82. With respect to Figure 4, and in particular controller 120-b, the patents state:

> The controller 120-*b* includes an adaptive encoding rate controller 405, a power controller 410, a write controller 415, a read controller 420, an age monitoring module 425, and an error monitoring module 430. The age monitoring module 425 may monitor an age associated with the flash memory 110-*b*. This may be a time since manufacture, a time since first use,

> an amount of use, or any other metric which corresponds to the aging of the flash memory 110-*b*. This monitoring may involve direct monitoring of the flash memory 110-*b* itself, or may be based on reports from the encoder 105-*b*, decoder 115-*b*, or other components of the system.
>
> The error monitoring module 430 may monitor an amount of errors associated with the flash memory 110-*b*. This monitoring may measure errors over a variety of time periods and metrics, and may be translated into an error rate. The monitoring may be performed on a per-sector (or per set of sectors) basis. A number of sampling and averaging techniques may be used. This monitoring may involve direct monitoring of the decoder 115-*b* itself, or may be based on reports from the decoder 115-*b* or other components of the system.

'700 patent, 7:38-57.

83. In concluding remarks, the patents state that "embodiments may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof." '700 patent, 10:26-28.

VII. ANALYSIS OF CERTAIN DISPUTED CLAIM TERMS

A. "error detection sub-module…"

84. I have formed certain opinions regarding the term "error detection sub-module …" appearing in independent claims 1, 15, and 17 as well as certain dependent claims. The claim terms are:

error detection sub-module configured to: receive a different one of the plurality of partially decoded data streams; detect whether a portion of the respective received stream contains an error; and forward the portion of	Claim 1

the respective received stream containing an error to an error correction module	
error detection sub-module [] configured to: detect whether a portion of the respective received stream contains an error; and forward the portion of the respective received stream containing an error to an error correction module of the decoder	Claim 15
error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error; and forward the portion of the respective received stream containing an error to an error correction module	Claim 17

85. My opinions below apply equally to the "error detection sub-module …" term as it appears in each of these claims.

86. I have been asked to consider whether the "error detection sub-module …" term in each claim, in the context of the claims themselves and the specification, would invoke in the mind of a POSITA at the time of invention (or after) a specific structure that performs each of the functions these sub-module is configured to perform, as identified in the chart above.

87. I have concluded that they would not.

88. The term "sub-module" would not be understood by POSITA as conveying any particular structure or class of structures. Rather, "sub-module" would be used in the context of the technology at issue, and elsewhere, synonymously with the expression "black box."

89. The prefix "error detection" imparts no structure and does not alter my conclusion that these terms would be understood as reciting no more than a "black box" in terms of structure—much less as disclosing a particular structure or class of structures—for

performing the functions identified in the chart above, including, for example, the function, "detect whether a portion of the respective received stream contains an error."

90. Further, I find no other language in claims 1, 15, and 17 that imparts structure to the "error detection sub-module …" for performing these functions.

91. I have examined the specification of the '700 patent to see if it provides its own definition of "error detection sub-module," one that includes specific structure for performing the functions attributable to these sub-modules, including detecting errors in received data streams. I have found no such definitions.

92. To the contrary, the specification, consistent with a POSITA's understanding of the term, treats "error detection sub-module" as a mere black box for performing certain functions and never describes an "error detection sub-module" having a particular structure or even class of structures.

93. For example, the '700 patent states, with reference to Figure 3 below: "The error detection module 210-*a* includes a number of error detection sub-modules 315…. Each error detection sub-module 315 may evaluate the respective stream to determine

whether a portion contains an error … [and] may forward the portion of the respective received stream containing any error….").

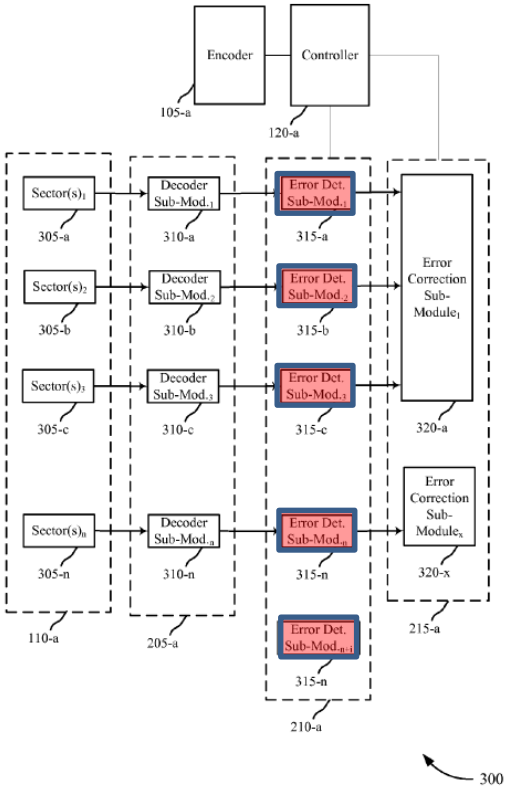


FIG. 3

'700 patent, FIG. 3 (the "error detection sub-modules 315" are annotated in red); *see also id.* at 6:14–42.

94. Consistently, the '700 patent states, with respect to "error detection module" sub-modules, and "error correction module" sub-modules that:

> These … sub-modules … may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs),

> and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

'700 patent, 5:62-6:8; *see also id*. 5:47-5:61.

95. A POSITA would not have understood this disclosure as defining a specific or sufficient structure for performing error detection or any other function. To the contrary, the disclosure recites generic components that amount to a black box having generic components merely capable of being arranged and programmed—in some manner nowhere discussed in the specification—to perform the specified functions.

96. Because it is my opinion that the "error detection sub-module…" term in claims 1, 15, and 17 convey no specific or sufficient structure to a POSITA for performing the functions enumerated in the chart above, and instead merely constitutes a black box in the context of the electrical arts containing non-descript circuitry and/or processor(s) executing software, I interpret the "error detection sub-module…" terms as reciting "means-plus-function" limitations.

97. As "means-plus-function" limitations, I have conducted a further analysis to determine whether the '700 patent would be understood by a POSTIA as describing adequate corresponding structure that is clearly linked or associated with each claimed function.

98. After careful review of the claims and specification of the '700 patent, I have concluded that it would not.

99. The passage of the '700 patent quoted above (5:62-6:8), which describes sub-modules broadly as being capable of being "implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions

in hardware," for example, does not describe adequate corresponding structure that is clearly linked or associated with each claimed function of the error detection sub-modules, including error detection. ASICs have no inherent structure, and certainly do not inherently perform error detection or any other data manipulation. Rather, the term refers essentially to a circuit implemented black box that may be designed to perform any number of functions.

100. The passage of the '700 patent quoted above (5:62-6:8), which alternately describes sub-modules broadly as being capable of being "performed by one or more other processing units (or cores), [or by] other types of integrated circuits … (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art" or by "instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors," for example, also does not describe adequate corresponding structure that is clearly linked or associated with each claimed function of the error detection sub-modules, including error detection.

101. These various alternatives recite general programmable circuitry, *e.g.*, "processing units" or "general or application-specific processors," that do not inherently perform the claimed functions of the error detection sub-modules, including error detection. Instead, they must be programmed to perform such functions, as acknowledged in the specification.

102. I understand that in such instances to satisfy the requirements of means-plus-function claiming, the specification must disclose the structure of the program being executed, *e.g.*, in the form of an algorithm.

103. I further understand that an algorithm is a step-by-step procedure for performing the claimed function. I understand that such an algorithm can be expressed in many forms, including flow charts, a series of specific steps, mathematical formula, prose, and so on. I understand that a restatement of the function itself in the specification is inadequate to disclose an algorithm for performing the claimed function. I understand that description of an algorithm or class of algorithms that places no limitations on how values are calculated, combined, or weighted is insufficient to make the bounds of the claim understandable.

104. The "error detection sub-module" of claim 1 performs three functions: (i) "receive a different one of the plurality of partially decoded data streams"; (ii) detect whether a portion of the respective received stream contains an error"; and (iii) "forward the portion of the respective received stream containing an error to an error correction module." The "error detection sub-modules" of claims 15 and 17 do not expressly include the "receive" function (though it appears to be implicitly included in these claims) but do require substantively the same "detect" and "forward" functions.

105. I have found no algorithms described in the '700 patent for performing any of these claimed functions. Rather, the patent specification mimics the functional claim language without offering any step-by-step procedure for performing these functions.

106. For example, in connection with Figure 5 of the '700 patent showing "a flowchart illustrating a method of decoding data from a flash memory according to various embodiments of the invention" ('700 patent, 2:14-16), the patent simply repeats certain claimed functions by stating for "block 515":

> At block 515, at each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error, and forward the portion of the respective received stream containing an error to an error correction module.

'700 patent, 8:52-58; *see also id*. at Fig. 5.

107. This purely functional sub-module description is repeated throughout the patent. *See, e.g.*, '700 patent, 6:16–23 ("As noted, the error detection module 210 may include a number of error detection sub-modules operating in parallel. Each (or a subset) of the error detection sub-modules may receive a different one of the data streams, and evaluate the respective stream to determine whether a portion of the stream contains an error. Each error detection sub-module may forward the portion of the respective received stream containing an error to the error correction module 215 …."), 6:61-67, Abstract, 1:35-39, 2:32-35.

108. None of these disclosures constitute any step-by-step procedure for performing the oft recited "receive," "detect" and "forward" functions of the "error detection sub-modules."

109. Nor have I found an algorithm that is clearly linked to each of the claimed functions in any other portion of the specification.

110. The specification's disclosure that "a number of different FEC schemes and codes … may be used in the flash memory system…." ('700 patent, 3:63-65), including "Hamming Code, with correction capacity of 1 bit and detection capability of 2," "Bose

Chaudhuri Hocqunghem (BCH) codes … including the binary BCH and non-binary BCH (Reed Solomon (RS)) codes," and "Convolutional Turbo Codes (CTCs), Turbo Product Codes (TPCs), and low density parity check codes (LDPCs)" ('700 patent, 4:7-24) also fails to inform a POSITA as to any specific structural implementation of the "error detection sub-modules."

111. These various error control codes merely represent, at a very high level, certain forward error correction coding technologies. Each relates, in general terms to different methods for computing and adding certain parity information to data to be stored in memory, *i.e.*, encoding, that can be used upon retrieving the data from memory to correct up to a certain number of errors that may have been introduced since the data was originally stored, or to estimate the code sequence or information bits from "soft" versions of the retrieved data. This disclosure in the specification is nothing more than a regurgitation of known categories of certain forward error correction coding technologies. Nothing about this disclosure conveys to a POSITA how to perform the function of "error detection."

112. None of the '700 patent's passing references to these exemplary FEC algorithms convey to a POSITA a circuit or program architecture sufficient to define an "error detection sub-module" that performs the recited "receive," "detect" and "forward" functions. For every single class of error control codes listed in the written description, there are multiple possible encoding and decoding schemes. As noted below, some of the cited error control schemes do not even reduce the received information to a binary stream prior to error correction, making "error detection" meaningless. Further, the implementation of error detection is dependent on numerous variables not specified in

the claims, including the specific encoding parameters chosen, data throughput and system response time requirements, cost, and power budget, to name a few.

113. In fact, the "Hamming Code" with "detection capability of 2" referred to in the specification, is more accurately referred to as an *extended* Hamming code. And, when using such codes for FEC, error correction and error detection functions are performed simultaneously, meaning that this FEC algorithm would not be understood as having any distinct "error detection sub-modules," let alone one having a specific structure.

114. Further, the Convolutional Turbo Codes ("CTC"), Turbo Product Codes ("TPC"), and Low Density Parity Check ("LDPC") codes referred to in the specification are used for error correction, not error detection, and thus convey no information to a POSITA about the structure and/or programming of the claimed "error detection sub-modules." I further note that turbo and LDPC decoders operate on "soft" values, and imply no mechanism whatsoever to a POSITA for a distinct error detection component.

115. Reference to the remaining codes would not be understood by a POSITA as providing any step-by-step procedure for performing the "error detection sub-module" "receive," "detect" and "forward" functions.

116. This lack of disclosure is even more conspicuous in view of the fact that the claims recite a plurality of data streams, each of which is sent to a separate error detection sub-module and there is no disclosure in the '700 patent of either an error detection algorithm for these schemes or of how any error detection algorithm is to be divided among sub-modules.

117. Further, implementation of error detection is dependent on numerous variables not specified in the claims, including the specific encoding parameters chosen, data

throughput and system response time requirements, cost, and power budget, to name a few.

B. "error correction module…"

118. I have formed certain opinions regarding the term "error correction module …" appearing in independent claims 1, 15, and 17 as well as certain dependent claims. The claim terms are:

error correction module … configured to correct the received portions of the respective received streams containing an error	Claim 1
correct, with the **error correction module** … the forwarded portions of the respective received streams containing an error.	Claim 15
correcting, with the **error correction module** … the forwarded portions of the respective received streams containing an error.	Claim 17

119. My opinions below apply equally to the "error correction module …" term as it appears in each of these claims.

120. I have been asked to consider whether the "error correction module …" term in each claim, in the context of the claims themselves and the specification, would invoke in the mind of a POSITA at the time of invention (or after) a specific structure that performs the function the "error correction module" is configured to perform—"[correct/correcting the [received/forwarded] portions of the respective received streams containing an error."

121. I have concluded that it would not.

122. The term "module" would not be understood by POSITA as conveying any particular structure or class of structures. Rather, "module," like the term "sub-module," would

be used in the context of the technology at issue, and elsewhere, synonymously with the expression "black box."

123. The prefix "error correction" imparts no structure and does not alter my conclusion that these terms would be understood as reciting no more than a "black box" in terms of structure—much less as disclosing a particular structure or class of structures—for performing the "[correct/correcting] …" function attributed to the "error correction module" in the claims.

124. Further, I find no other language in claims 1, 15, and 17 that imparts structure to the "error correction module …" for performing these functions. All that the claims recite is that the "error correction module," whatever its structure may be, is "physically separate from [the/an] error detection module."

125. I have also examined the specification of the '700 patent to see if it provides its own definition of "error correction module," one that includes specific structure for performing the claimed "correct/correcting [of] error[s]." I have found no such definitions.

126. To the contrary, the specification, consistent with a POSITA's understanding of the term, treats "error correction module" as a mere black box and never describes the term "error correction module" as having a particular structure or even class of structures.

127. For example, the '700 patent states, with reference to Figure 2 below: "The flash memory decoder 115-*a* includes a decoder module 205, an error detection module 210, and an error correction module 215…." '700 patent, 3:53–55.

128. This can be seen, for example, in Figure 2:

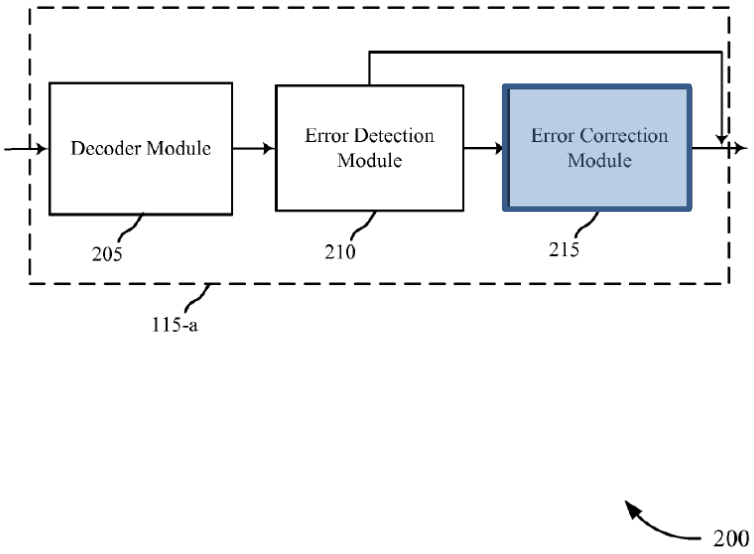


FIG. 2

'700 patent, FIG. 2 (the "error correction module 215" is annotated in blue); *see also id*. at FIG 3, 6:29-38 ("FIG. 3 is a block diagram illustrating an example of an architecture for a flash memory decoder system 300 more particularly illustrating error detection and correction sub-modules. The flash memory decoder system 300 may, for example, be the system 100 of FIG. 1. The flash memory decoder system 300 includes flash memory 110-a, a decoder module 205-a, an error detection module 210-a, an error correction module 215-a, a controller 120-a, and an encoder 105-a. Each of these components may be in communication with each other.").

129. The '700 patent states, with respect to Figure 3 presented above:

> The error correction module 215-a includes a number of error correction sub-modules 320, each error correction sub-module 320 responsible for handling the errors from a number of error detection sub-modules 315 (e.g., error correction sub-module 320 may correct errors from error detection

> sub-modules 315-a, -b, and -c). Error correction sub-modules 320 may correct the received portions of the respective received streams containing an error. Each error correction sub-module 320 may receive portions of streams with errors, and these portion may have been detected in parallel.

'700 patent, 6:67-7:10.

130. This disclosure at most indicates to a POSITA that the black box that is the "error correction module" can be subdivided into a number of black boxes. A POSITA would not understand this disclosure as defining the "error correction module," or its sub-modules, as having a specific or particular structure or even class of structures.

131. Consistently, the '700 patent states, with respect to "error detection module," "error correction module," and their respective sub-modules, that:

> These components and sub-modules therein may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

'700 patent, 5:62-6:8; *see also id*. 5:47-5:61.

132. A POSITA would not have understood this disclosure as defining a specific or sufficient structure for performing error correction or any other function. To the

contrary, the disclosure recites generic components that amount to a black box having generic components merely capable of being arranged and programmed—in some manner nowhere discussed in the specification—to perform error correction.

133. Because it is my opinion that the "error correction module…" term in claims 1, 15, and 17 convey no specific or sufficient structure to a POSITA for performing the claimed "[correct/correcting] [of] error[s]," and instead merely constitutes a black box in the context of the electrical arts containing non-descript circuitry and/or processor(s) executing software, I interpret these "error correction module…" terms as reciting "means-plus-function" limitations.

134. As "means-plus-function" limitations, I have conducted a further analysis to determine whether the '700 patent would be understood by a POSITA as describing adequate corresponding structure that is clearly linked or associated with each claimed function ascribed to the "error correction modules."

135. After careful review of the claims and specification of the '700 patent, I have concluded that it would not.

136. The passage of the '700 patent quoted above (5:62-65), which describes modules and sub-modules broadly as being capable of being "implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware," for example, does not describe adequate corresponding structure that is clearly linked or associated with each claimed function of the error correction modules. As I explained above, ASICs have no inherent structure, and certainly do not inherently perform error correction or any other data

manipulation. Rather, the term refers essentially to a circuit-implemented black box that may be designed to perform any number of functions.

137. The passage of the '700 patent quoted above (5:66-6:8), which alternately describes modules and sub-modules broadly as being capable of being "performed by one or more other processing units (or cores), [or by] other types of integrated circuits … (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art" or by "instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors," for example, also does not describe adequate corresponding structure that is clearly linked or associated with the error correction function of an "error correction module."

138. As I explained above, these various alternatives recite general programmable circuitry, *e.g.*, "processing units" or "general or application-specific processors," that do not inherently perform error correction. This circuitry must be programmed to perform such function, as acknowledged in the specification.

139. As I noted above, it is my understanding that in such instances, to satisfy the requirements of means-plus-function claiming, the specification must disclose the structure of the program being executed, *e.g.*, in the form of an algorithm reciting a step-by-step procedure for performing the claimed function.

140. I understand that such an algorithm can be expressed in many forms, including flow charts, a series of specific steps, mathematical formula, prose, and so on, but a restatement of the function itself in the specification is inadequate and that description of an algorithm or class of algorithms that places no limitations on how values are

calculated, combined, or weighted is insufficient to make the bounds of the claim understandable.

141. The "error correction module" appearing in each of claims 1, 15, and 17 performs the function of "[correct/correcting the [received/forwarded] portions of the respective received streams containing an error."

142. I have found no particular or sufficient algorithm described in the '700 patent for performing this function. Rather, the patent specification mimics the functional claim language without offering any step-by-step procedure for performing error correction.

143. For example, in connection with Figure 5 of the '700 patent showing "a flowchart illustrating a method of decoding data from a flash memory according to various embodiments of the invention" ('700 patent, 2:14-16), the patent simply repeats certain claimed functions by stating:

> At block 520, at the error correction module physically separate from the error detection sub-modules, the forwarded portions of the respective received streams containing an error are corrected.

'700 patent, 8:58-61; *see also id*. at Fig. 5.

144. This purely functional sub-module description is repeated throughout the patent. *See, e.g.*, '700 patent, 6:23-25 ("The error correction module 215 corrects the received portions of the respective received streams containing an error."), Abstract, 1:39–41, 2:35–37, 3:60–62, 6:67-7:10.

145. None of these disclosures constitute any step-by-step procedure for performing the recited error correction.

146. Nor have I found a specific, step-by-step, or otherwise sufficient algorithm for performing the recited error correction in any other portion of the specification.

147. The specification's disclosure that "a number of different FEC schemes and codes … may be used in the flash memory system…." ('700 patent, 3:63-65), including "Hamming Code, with correction capacity of 1 bit and detection capability of 2," "Bose Chaudhuri Hocqunghem (BCH) codes … including the binary BCH and non-binary BCH (Reed Solomon (RS)) codes," and "Convolutional Turbo Codes (CTCs), Turbo Product Codes (TPCs), and low density parity check codes (LDPCs)" ('700 patent, 4:7-24) also fails to inform a POSITA as to any specific structural implementation of the "error correction modules."

148. These various error control codes merely represent, at a very high level, certain forward error correction coding technologies. Each relates, in general terms to various methods for computing and adding certain parity information to data to be stored in memory, *i.e.*, encoding, that can be used upon retrieving the data from memory to correct up to a certain number of errors that may have been introduced since the data was originally stored.

149. None of the '700 patent's passing references to these exemplary FEC algorithms convey to a POSITA a circuit or program architecture sufficient to provide a step-by-step algorithm for programming an "error correction module" to correct errors in the received/retrieved "encoded data" of claims 1, 15, and 17. These disclosures are nothing more than a regurgitation of known categories of certain forward error correction coding technologies.

150. At most, each of these exemplary FEC coding schemes suggests a class of algorithms for performing error correction, the specific implementation of which remains unspecified and not ascertainable to a POSITA. For every single class of error control codes listed in the written description, there are multiple possible encoding and decoding schemes. Furthermore, the problem of creating separate error detection and correction schemes based on the cited codes remains an unsolved mystery. As noted, some of the cited error control schemes do not even reduce the received information to a binary stream prior to error correction, making "error detection" meaningless. Further, the implementation of error correction, like error detection, is dependent on numerous variables not specified in the claims, including the specific encoding parameters chosen, data throughput and system response time requirements, cost, and power budget, to name a few.

151. In addition, even had the '700 patent provided a specific and sufficient algorithm for performing error correction on data encoded with any of these algorithms, this algorithm would not, in general, work on data encoded by another scheme, and claims 1, 15, and 17 do not appear to restrict the encoding format of the received/retrieved "encoded data" to any one of the exemplary FEC schemes, meaning that even disclosure of an error correction algorithm for one or more of these schemes would not be sufficient to decode the recited "encoded data."

C. "error monitoring module…"

152. I have formed certain opinions regarding the term "error monitoring module …" appearing in dependent claims 6, 7, 11, and 12. The claim terms are:

error monitoring module … configured to monitor a rate of errors from the error detection module	Claims 6 and 11
error monitoring module … configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory,	Claim 7 and 12

153. My opinions below apply equally to the "error monitoring module …" terms as they appear in each of these claims.

154. I have been asked to consider whether the "error monitoring module …" terms in each claim, in the context of the claims themselves and the specification, would invoke in the mind of a POSITA at the time of invention (or after) a specific structure that performs the functions these modules are configured to perform, namely monitor a rate of errors from the error detection module [for each of a plurality of sectors of the flash memory]," as identified in the chart above.

155. I have concluded that they would not.

156. As I stated above, the term "module" would not be understood by POSITA as conveying any particular structure or class of structures. Rather, "module" would be used in the context of the technology at issue, and elsewhere, synonymously with the expression "black box."

157. The prefix "error monitoring" imparts no structure and does not alter my conclusion that these terms would be understood as reciting no more than a "black box" in terms of structure—much less as disclosing a particular structure or class of structures—for performing the error monitoring functions identified in the chart above.

158. Further, while claims 6, 7, 11, and 12 recite an "error monitoring module …" that is "communicatively coupled with the error detection module," I find no language in claims 6, 7, 11 and 12 that imparts structure to the "error monitoring module …" itself for performing these functions.

159. I have examined the specification of the '700 patent to see if it provides its own definition of "error monitoring module," one that includes specific structure for performing the error monitoring functions. I have found no such definitions.

160. To the contrary, the specification, consistent with a POSITA's understanding of the term, treats "error monitoring module" as a mere black box for performing error monitoring functions and never describes a "error monitoring module" having a particular structure or even class of structures.

161. The '700 patent depicts an "error monitoring module" in Figure 4 below, which shows a flash memory decoder system 400 that may be an example of the system 100 of Figure 1 of the '700 patent. ''700 Patent, 7:27-34.

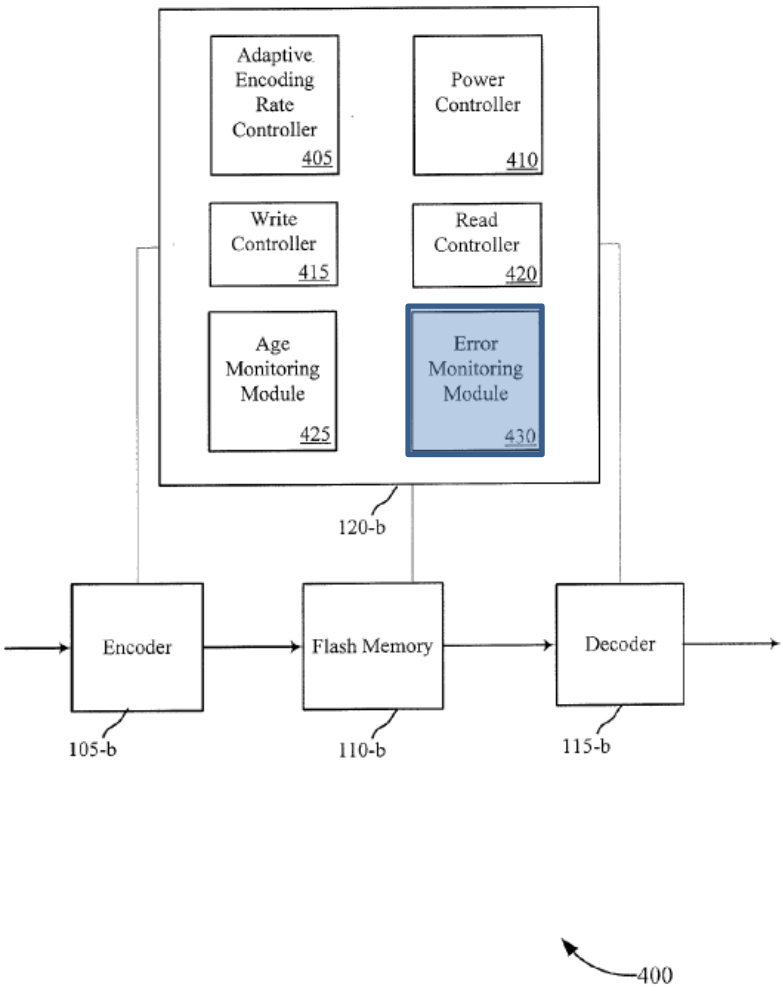


FIG. 4

'700 patent, FIG. 4 (the "error monitoring module 430" is annotated in blue).

162. The '700 patent states, with reference to Figure 4 below:

> The controller 120-b includes … an error monitoring module 430.…
>
> The error monitoring module 430 may monitor an amount of errors associated with the flash memory 110-b. This monitoring may measure errors over a variety of time periods and metrics, and may be translated into

> an error rate. The monitoring may be performed on a per-sector (or per set of sectors) basis. A number of sampling and averaging techniques may be used. This monitoring may involve direct monitoring of the decoder 115-b itself, or may be based on reports from the decoder 115-b or other components of the system.

'700 Patent, 7:38-57.

163. These disclosures do not convey to a POSITA a specific structure directly linked to the recited error monitoring function.

164. Consistently, the '700 patent states, with respect to its various components, including decoder 115 of Figure 1, of which the system 400 of Figure 4 containing error monitoring module 430 is an example, that:

> [Decoder 115] may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

'700 patent, 3:31-45, 5:62-6:8; *see also id*. 5:62-6:8.

165. A POSITA would not have understood this disclosure as defining a specific or sufficient structure for performing error detection or any other function. To the contrary, the disclosure recites generic hardware that amounts to a black box having

generic components merely capable of being arranged and programmed—in some manner nowhere discussed in the specification—to perform the specified error correction.

166. Because it is my opinion that the "error monitoring module…" term in claims 6, 7, 11, and 12 convey no specific or sufficient structure to a POSITA for performing the recited error correction functions, and instead merely constitutes a black box in the context of the electrical arts containing non-descript circuitry and/or processor(s) executing software, I interpret the "error detection sub-module…" terms as reciting "means-plus-function" limitations.

167. As "means-plus-function" limitations, I have conducted a further analysis to determine whether the '700 patent would be understood by a POSTIA as describing adequate corresponding structure that is clearly linked or associated with each claimed function.

168. After careful review of the claims and specification of the '700 patent, I have concluded that it would not.

169. The passage of the '700 patent quoted above (3:31-36), which describes system components broadly as being capable of being "implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware," for example, does not describe adequate corresponding structure that is clearly linked or associated with the error monitoring functions of the claimed error monitoring modules. As I explained above, ASICs have no inherent structure, and certainly do not inherently perform error monitoring or any other data manipulation. Rather, the term refers essentially to a circuit-implemented black box that may be designed to perform any multitude of functions.

170. The passage of the '700 patent quoted above (3:36-45), which alternately describes system components as being capable of being "performed by one or more other processing units (or cores), [or by] other types of integrated circuits … (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art" or by "instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors," for example, also does not describe adequate corresponding structure that is clearly linked or associated the claimed functions of the error monitoring modules.

171. As I explained above, these various alternatives recite general programmable circuitry, *e.g.*, "processing units" or "general or application-specific processors," that do not inherently perform the claimed functions of the error monitoring modules. This circuitry must be programmed to perform such functions, as acknowledged in the specification.

172. As I noted above, it is my understanding that in such instances, to satisfy the requirements of means-plus-function claiming, the specification must disclose the structure of the program being executed, *e.g.*, in the form of an algorithm reciting a step-by-step procedure for performing the claimed function.

173. I understand that such an algorithm can be expressed in many forms, including flow charts, a series of specific steps, mathematical formula, prose, and so on, but a restatement of the function itself in the specification is inadequate and that description of an algorithm or class of algorithms that places no limitations on how values are

calculated, combined, or weighted is insufficient to make the bounds of the claim understandable.

174. The "error monitoring module" appearing in each of claims 6, 7, 11, and 12 performs the function of "configured to monitor a rate of errors from the error detection module [for each of a plurality of sectors of the flash memory]."

175. I have found no particular or sufficient algorithm described in the '700 patent for performing this function. Rather, the patent specification mimics the functional claim language without offering any step-by-step procedure for performing error correction.

176. For example, in connection with Figure 4 of the '700 patent, as quoted above the patent simply states:

> The error monitoring module 430 may monitor an amount of errors associated with the flash memory 110-b. This monitoring may measure errors over a variety of time periods and metrics, and may be translated into an error rate. The monitoring may be performed on a per-sector (or per set of sectors) basis. A number of sampling and averaging techniques may be used. This monitoring may involve direct monitoring of the decoder 115-b itself, or may be based on reports from the decoder 115-b or other components of the system.

'700 patent, 8:49-57; *see also id*. at Fig. 4.

177. None of these disclosures would be understood by a POSITA as constituting any step-by-step procedure for performing the recited error monitoring. Nor have I found a specific, step-by-step, or otherwise sufficient algorithm for performing the recited error correction in any other portion of the specification. To the contrary, this disclosure

refines the error monitoring function, *e.g.*, the "monitoring may measure errors over a variety of time periods and metrics," but fails to provide an error monitoring algorithm.

178. In fact, the specification fails to define what "errors from the error detection module" are even being monitored, exacerbating the effort to find corresponding structure. For example, the '700 patent does not state whether these claimed errors represent failures of the error detection module itself, *e.g.*, where this module fails to detect one or more errors that do exist in the data received/retrieved, or detects errors that do not exist, or whether the claimed errors relate to one or more types of errors in the underlying received/retrieved encoded data, *e.g.*, inaccurate data bits, inaccurate parity bits, missing bits, etc….

D. "error correction sub-module…"

179. I have formed certain opinions regarding the term "error correction sub-module …" appearing in independent claims 1 and 13 of the '347 patent as well as certain dependent claims. The claim terms are:

processing, using at least a first **error correction sub-module**, the data stream to correct errors in the data stream associated with the flash memory	Claim 1
process the data stream to correct errors in the data stream associated with the flash memory using at least a first **error correction sub-module**;	Claim 13
a second **error correction sub-module** arranged in parallel with the first error correction sub-module for subsequent data stream processing.	Claims 1 and 13

180. My opinions below apply equally to both the first and second "error correction sub-module …" terms as they appear in each of these claims and closely align with my opinions respecting the "error correction module …" terms of the '700 patent.

181. I have been asked to consider whether the "error correction sub-module …" term in each claim, in the context of the claims themselves and the specification, would invoke in the mind of a POSITA at the time of invention (or after) a specific structure that performs the function the "error correction sub-module" is configured to perform—"[processing/process] … the data stream to correct errors in the data stream associated with the flash memory."

182. I have concluded that it would not.

183. As I have explained above, the term "sub-module" would be used in the context of the technology at issue, and elsewhere, synonymously with the expression "black box."

184. The prefix "error correction" imparts no structure and does not alter my conclusion that these terms would be understood as reciting no more than a "black box" in terms of structure.

185. Further, I find no other language in claims 1 and 13 that imparts structure to the "error correction sub-module …" for performing these functions.

186. I have also examined the specification of the '347 patent to see if it provides its own definition of "error correction sub-module," one that includes specific structure for performing the claimed "[processing/process] … the data stream to correct errors in the data stream associated with the flash memory." As with the "error correction module …" of the '700 patent, I have found no such definitions.

187. To the contrary, like the "error correction sub-module …" of the '700 patent, the essentially identical specification of the '347 patent treats "error correction sub-module" as a mere black box and never describes the term "error correction sub-module" as having a particular structure or even class of structures.

188. For example, the ’347 patent states, with reference to Figure 3 below:

> The error correction module 215-a includes a number of error correction sub-modules 320, each error correction sub-module 320 responsible for handling the errors from a number of error detection sub-modules 315 (e.g., error correction sub-module 320 may correct errors from error detection sub-modules 315-a, -b, and -c). Error correction sub-modules 320 may correct the received portions of the respective received streams containing an error. Each error correction sub-module 320 may receive portions of streams with errors, and these portion may have been detected in parallel.

’347 patent, 7:2–12; *see also id*. at 6:25–40.

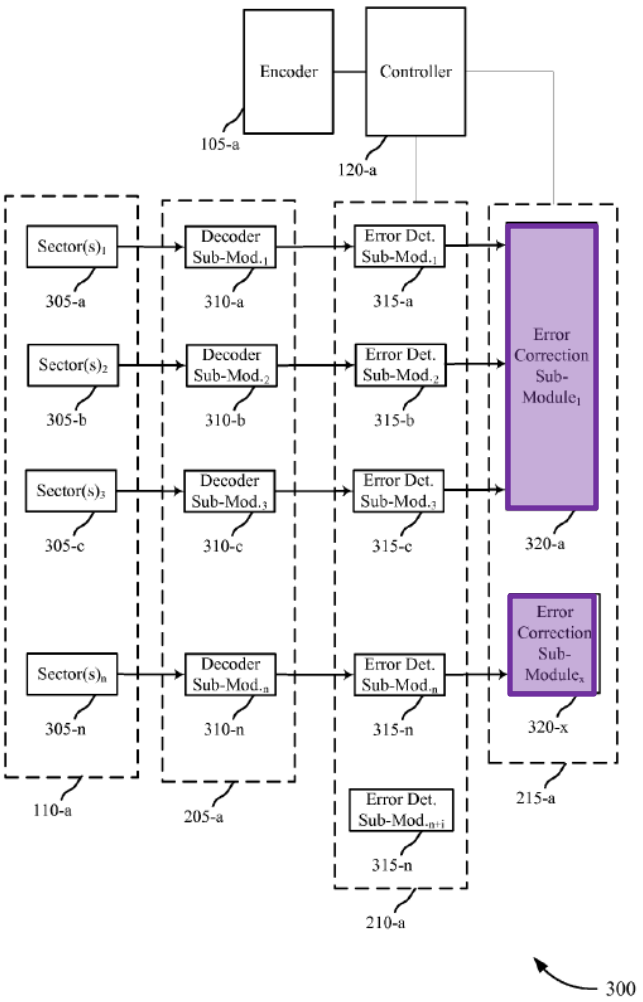


FIG. 3

'347 patent, FIG. 3 (the "error correction sub-modules 320" are annotated in purple).

189. This disclosure at most indicates to a POSITA that the black box that is the "error correction sub-module" can be subdivided into a number of black boxes. A POSITA would not understand this disclosure as defining the "error correction sub-module," as having a specific or particular structure or even class of structures.

190. Consistently, the '347 patent, like the '700 patent, states, with respect to "error detection module," "error correction module," and their respective sub-modules, that:

> These components and sub-modules therein may, individually or collectively, be implemented with one or more Application Specific

> Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

'347 patent, 5:64-6:10; *see also id*. 5:49-5:63.

191. A POSITA would not have understood this disclosure as defining a specific or sufficient structure for performing error correction or any other function. To the contrary, the disclosure recites generic components that amount to a black box having generic components merely capable of being arranged and programmed—in some manner nowhere discussed in the specification—to perform error correction.

192. Because it is my opinion that the "error correction sub-module…" term in claims 1 and 13 convey no specific or sufficient structure to a POSITA for performing the claimed function of "[processing/process] … the data stream to correct errors in the data stream associated with the flash memory," and instead merely constitutes a black box in the context of the electrical arts containing non-descript circuitry and/or processor(s) executing software, I interpret these "error correction sub-module…" terms as reciting "means-plus-function" limitations.

193. As "means-plus-function" limitations, I have conducted a further analysis to determine whether the '347 patent would be understood by a POSTIA as describing adequate

corresponding structure that is clearly linked or associated with the claimed error correcting function ascribed to the "error correction sub-modules."

194. After careful review of the claims and specification of the '347 patent, I have concluded that it would not.

195. The passage of the '347 patent quoted above (5:64-67), which describes modules and sub-modules broadly as being capable of being "implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware," for example, does not describe adequate corresponding structure that is clearly linked or associated with each claimed error correction function of the "error correction sub-modules." As I explained above, ASICs have no inherent structure, and certainly do not inherently perform error correction or any other data manipulation. Rather, the term refers essentially to a circuit-implemented black box.

196. The passage of the '347 patent quoted above (6:1-6:10), which alternately describes modules and sub-modules broadly as being capable of being "performed by one or more other processing units (or cores), [or by] other types of integrated circuits … (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art" or by "instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors," for example, also does not describe adequate corresponding structure that is clearly linked or associated with the error correction performed by the error correctio sub-modules.

197. As I explained above with respect to the other module and sub-module terms, these various alternatives recite general programmable circuitry that does not inherently perform any function.

198. As I noted above, it is my understanding that in such instances, to satisfy the requirements of means-plus-function claiming, the specification must disclose the structure of the program being executed, *e.g.*, in the form of an algorithm reciting a step-by-step procedure for performing the claimed function.

199. I understand that such an algorithm can be expressed in many forms, including flow charts, a series of specific steps, mathematical formula, prose, and so on, but a restatement of the function itself in the specification is inadequate and that description of an algorithm or class of algorithms that places no limitations on how values are calculated, combined, or weighted is insufficient to make the bounds of the claim understandable.

200. The "error correction sub-module" appearing in each of claims 1 and 13 performs the function of "[processing/process] … the data stream to correct errors in the data stream associated with the flash memory."

201. I have found no particular or sufficient algorithm described in the '347 patent for performing this function. Rather, the patent specification mimics the functional claim language without offering any step-by-step procedure for performing error correction.

202. For example, the '347 patent states, with reference to Figure 3 below:

> The error correction module 215-a includes a number of error correction sub-modules 320, each error correction sub-module 320 responsible for handling the errors from a number of error detection sub-modules 315 (e.g.,

> error correction sub-module 320 may correct errors from error detection sub-modules 315-a, -b, and -c). Error correction sub-modules 320 may correct the received portions of the respective received streams containing an error. Each error correction sub-module 320 may receive portions of streams with errors, and these portion may have been detected in parallel.

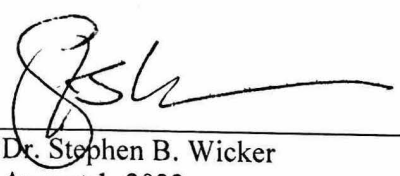
'347 patent, 7:2–12; *see also id.* at 6:25–40.

203. As I explained with respect to the "error correction modules" of the '700 patent, the '347 patent specification's identical disclosure that "a number of different FEC schemes and codes … may be used in the flash memory system…." ('347 patent, 3:65-67), including "Hamming Code, with correction capacity of 1 bit and detection capability of 2," "Bose Chaudhuri Hocqunghem (BCH) codes … including the binary BCH and non-binary BCH (Reed Solomon (RS)) codes," and "Convolutional Turbo Codes (CTCs), Turbo Product Codes (TPCs), and low density parity check codes (LDPCs)" ('347 patent, 4:9-26) also fails to inform a POSITA as to any specific structural implementation of the "error correction sub-modules."

VIII. CONCLUSION

204. I reserve the right to supplement my opinions in the future to respond to any arguments raised by Viasat or opinions offered by its expert(s) and to take into account new information that becomes available to me.

205. I declare under penalty of perjury of the laws of the United States that the foregoing is true and correct.

By: 

Dr. Stephen B. Wicker
August 1, 2022

Exhibit A

DR. STEPHEN B. WICKER

Professor
School of Electrical and Computer Engineering
Cornell University

EDUCATION

Ph.D.	Electrical Engineering University of Southern California	1987
M.S.E.E.	Electrical Engineering Purdue University	1983
B.S.E.E.	Electrical Engineering University of Virginia	1982

EMPLOYMENT HISTORY

Cornell University, Ithaca New York	
School of Electrical Engineering	
Associate Director for Research	2000 - 2003
Professor	1999 -
Associate Professor	1996-1999
Georgia Institute of Technology, Atlanta, Georgia	
School of Electrical and Computer Engineering	
Associate Professor	1992-1996
Assistant Professor	1987-1992
Hughes Aircraft, El Segundo, California, Information Sciences Department, System Laboratories, Space and Communications	
Staff Engineer	1983-1987
Bell Laboratories, Network Architecture Research Group Columbus, Ohio	1982

EXPERIENCE SUMMARY

Professor Wicker teaches and conducts research in wireless information networks, secure networks, packet-switched computer networks, and digital telephony. His research has focused on the development and application of advanced technologies to adaptive networks. Current interests include privacy-aware design practices for wireless networks and self-configuring sensor networks for disaster recovery, infrastructure monitoring, and national security. Other interests include secure anonymous networking, the behavior of complex systems, phase transitions in NP-hard problems, and the evolution of the nation's telecommunications networks.

Professor Wicker is the Cornell Principal Investigator for the TRUST Science and Technology Center – a National Science Foundation center dedicated to the development of technologies for securing the nation's critical infrastructure.

In 2010 Professor Wicker testified before the Congressional Committee on Science and Technology and was appointed to the Air Force Scientific Advisory Board. He is a Fellow of the IEEE.

Technical Duties at Hughes Aircraft included the following:

1. Principal System Engineer for advanced military satellite communications, new business.
2. Team leader and principal author of study examining the use of 60 and 94 GHz monolithic arrays in satellite cross-links.
3. Team leader and principal author of study examining the use of High Electron Mobility Transistor (HEMT) devices in frequency synthesizers for frequency hopped communication systems.
4. Responsible for analysis, design, and production of 800 Mbps demod-remod SQPSK receiver.
5. Responsible for analysis and design of several receivers and digital signal processors for various military satellite programs.
6. Conducted analysis and simulation of MILSTAR direct digital frequency synthesizers.

Technical Duties at Bell Laboratories included the development of synchronous protocols for a packet switch (no. 2 STP).

CONSULTING

- Mitre Corporation., Eatontown, NJ. 1997 - 2005
  - Turbo Error Control for Wireless Applications.
- Motorola Inc. Advanced Mobile Messaging Division 1997 – 1998
  - Wireless Networking
- Digital Technics Inc., Baltimore, MD. 1995 - 1997
  - Design of SS7/SONET/ATM interface for telephone switch.
- Integrated Device Technology, Santa Clara, CA. 1995 - 1996
  - Development of Reed-Solomon error control chip for high-speed mass memory applications.
- Lockheed Sanders, Avionics Division, Nashua, N.H. 1994 - 1995
  - Development of error control chips for magnetic recording in space applications.
- Mobile Telecommunication Technologies, Jackson, MS. 1993 - 1998
  - Design and analysis of mobile networks for paging and data transfer, bulk data transfer using frame relay.
- Al-Elm Research and Development Corp., Raleigh, N.C. 1992 - 1994
  - Design and development of advanced digital voice and FAX encryption techniques.
- Intellivision, Atlanta, GA. 1992 - 1993
  - Design and development of automated telephone switching equipment.
- Unisys Corporation, San Jose, CA. 1991 - 1992
  - Design and development of error control algorithms for internodal communication in multiprocessing computer systems.
- II Morrow Inc., UPS Technical Systems, Salem, OR. 1990 - 1992
  - Analysis, design, and development of error control systems for mobile radio networks.
- Charter Leasing Corporation, Richmond, VA. 1990 - 1993

- Analysis and design of digital switching systems for commercial telephony.

CURRICULUM DEVELOPMENT

- Developed and implemented a course for Freshmen entitled "Wiretaps to Facebook: Security and Privacy in Information Networks" for the College of Engineering, Cornell University, Ithaca, New York (Fall 2010).

- Developed and implemented a course for Juniors entitled "Networks and Systems" for the School of Electrical Engineering, Cornell University, Ithaca, New York (Spring 2005).

- Developed and implemented a course for Seniors entitled "Artificial Intelligence and Expert Systems for Telecommunications Networks" for the School of Electrical Engineering, Cornell University, Ithaca, New York (Spring 1998).

- Developed and implemented a course for Freshmen entitled "Introduction to Telecommunications" for the College of Engineering, Cornell University, Ithaca, New York (Spring 1997).

- Developed and implemented a graduate course in Cryptography and Data Security for the School of Electrical Engineering, Cornell University, Ithaca, New York (Fall 1996).

- Academic Coordinator, Georgia Tech - Lorraine, Metz, France, September 1990 - March 1992.

- Developed and implemented two graduate courses in Error Control Coding and one graduate course in Cryptography and Data Security for the School of Electrical Engineering, Georgia Institute of Technology, Atlanta, Georgia.

- Developed and taught numerous short courses on digital communication systems, wireless information networks, error control, and cryptology.

PH. D. STUDENTS (GRADUATED)

Cornell University

- **Daniel Lee** ("Reliable and Energy-Efficient Wireless Sensor Networks for Mobile Healthcare Systems," graduated Summer 2011)
- **Nathan Karst** ("Combinatorial Designs For Key Distribution And Secure Re-Keying In Group Communication Systems," graduated Summer 2011)
- **Sergio Bermudez** ("Analysis of Topological Properties of Random Wireless Sensor Networks," graduated Summer 2010)
- **Mikhail Lisovich** ("Mobility And Privacy: Exploring Technical And Social Issues In Emerging Pervasive Sensor Networks," graduated Spring 2010)

- **Michael Eoin Buckley** (“Side Information Inference For Turbo Code Based Systems,” graduated Fall 2009)
- **Coalton Bennett** (“Secure Data Reporting for Demand Response Systems,” graduated Fall 2009)
- **Ania Kacewicz** (“Coding Theory for Security and Reliability in Wireless Networks,” graduated Fall 2009)
- **Phillip Kuryloski** (“Design Strategies For Human Centered Sensor Networks,” graduated Spring 2009)
- **Sameer Pai**, (“Co-Design Of Sensor Networking Technology And Privacy Policy,” graduated Spring 2008)
- **Hui Qu**, (“Co-Designed Localization And Geographic Routing Algorithm For Sensor Networks,” graduated Spring 2008)
- **Christina Tavoularis**, (“Event Detection and Queueing in Wireless Sensor Networks,” Graduated Fall 2006)
- **Hazer Inaltekin**, (“Game Theoretic Mac Protocol Design And Interference Analysis For Wireless Networks,” Graduated Spring 2006)
- **Xin Zhang**, (“Distributed Source Coding in Sensor Networks,” graduated Spring 2006)
- **Martin Roth**, (“TERMITE: A Swarm Intelligent Routing Algorithm for Mobile Wireless Ad Hoc Networks,” graduated Winter 2005)
- **Prince Samar**. (“Optimizing Protocols for Mobility in Ad Hoc Networks,” graduated Summer, 2004)
- **Yasser Mourtada**. (“Content-Aware Routing Schemes,” graduated Summer, 2004)
- **Allen MacKenzie**. (“Game Theoretic Analysis of Medium Access Control Protocols,” graduated Spring, 2003)
- **Ewald Hueffmeier, Jr**. (Applied Mathematics - Turbo Decoding Architectures and Algorithms for Wireless Data Systems, graduated Summer, 2002)
- **Xie Xi** (AI and Expert Systems for Random Access Protocols, graduated Summer, 2002)
- **Bhaskar Krishnamarchari** ("Complexity and Phase Transitions in Wireless Networks," graduated Spring, 2002)
- **Sarah Spence** ("Subfield Subcodes of Reed-Solomon Codes," graduated Spring, 2002)
- **Eric Sakk** ("Wavelets Based on Reed-Muller Coding," graduated Spring, 2002)
- **Frederic Fontaine** ("Iterative Trellis Decoding for Block Codes," graduated Summer, 1999)
- **Saejoon Kim** (“Belief Propagation, Parameter Estimation, and Issues in Turbo Decoding,” graduated Summer 1998)

Georgia Tech

- **Andreas Yankopolus**. (“Adaptive Error Control for Wireless Multimedia"), graduated Winter, 2004)
- **James Kosmach** (“Soft Decision Decoding for Wireless Mobile Systems,” graduated Fall. 1998)

- **Amjad Luna** ("DSP Implementation of Advanced Decoder Architectures," graduated Winter, 1998
- **Jong-Il Park** ("Turbo Equalization Algorithms," graduated Winter, 1998)
- **Thomas Tapp** ("Advanced Error Control Systems for Mobile Messaging Systems," graduated Summer, 1996)
- **Mahdi Zaidan** ("Tree Structure Trellis Codes," graduated Spring, 1996)
- **Xiao-An Wang** ("Trellis-Based Decoders and Neural Network Implementations," graduated Winter, 1996)
- **Ahmed El-Rifai** ("Application of Linear Block Codes to the McEliece Cryptosystem," graduated Fall, 1995)
- **Miin-Jong Hao** ("Performance Evaluation of Practical FSK, CPFSK, and ASK Detection Schemes for Coherent Optical Fiber Communication Systems," graduated Summer, 1995)
- **Slim Souissi** ("Adaptive Packet Combining in CDMA Systems," graduated Summer, 1994)
- **Deidre Williams** ("Key Management in the McEliece Cryptosystem," graduated Summer, 1994)
- **Lars Rasmussen** ("Trellis Coded Adaptive Rate Hybrid-ARQ Protocols over AWGN and Slowly Fading Rician Channels," graduated Summer 1993)
- **Mohssen Alabbadi** ("Integration of Error Correction, Encryption, and Signature Using Linear Error-Correcting Block Codes," graduated Summer 1993)
- **Michael Bartz** ("Soft Decision Decoders Based on Artificial Neural Networks," graduated Summer 1992)
- **Michael Rice** ("Adaptive Error Control Over Slowly Varying Channels," graduated Spring 1991)
- **Bruce Harvey** ("Adaptive Rate Convolutional Coding Using the Viterbi Decoder," graduated Spring 1991)

PH.D. STUDENTS (IN PROGRESS)

- **Daniel Lee** (Cellular Information Systems)
- **Nathan Karst** (Design Theory)
- **Dipayan Ghosh** (Smart Grid/Demand Response Systems)

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- Wicker, S. B. and Welch, L. R., “The Geometry of MDS Codes,” *Proceedings of the 1987 IEEE Pacific Rim Conference for Communications, Computers, and Signal Processing*, Victoria, British Columbia, pp. 89 - 92, June 4, 1987.

Invited Conference Papers

- Wicker, S. B., "Markov Chains, Error Control, and the Advent of Turbo Coding," IMA Workshop on Codes, Systems and Graphical Models, Minneapolis, MN, August 2-13, 1999.

- Buckley, M. E. and Wicker, S. B., " Optimization, Neural Networks, and Turbo Decoding," *Proceedings of the Fifth International Symposium on Communication Theory and Applications*, Ambleside, U. K., July 12 - 16, 1999.

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- Wicker, S. B., “Error Control in Space Applications,” 1995 Central Section Meeting of the American Mathematical Society, Chicago, Illinois, March 24 - 25, 1995.

- Wicker, S. B., “Error Control Techniques for Voice and Data Communications over Cellular Mobile Channels,” *Proceedings of the Allerton Conference on*

Communication, Control, and Computing, pp. 444 - 453, September 28 – 30, 1994.

- Wicker, S. B. and Alabbadi, M., "Susceptibility of Digital Signature Schemes Based on Error-Correcting Codes to Universal Forgery," Workshop on Information Protection, Moscow, Russia, December 6 - 9, 1993.

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Invited Seminar Presentations

- Vanderbilt University, March 2009
- Carnegie Mellon University, April 2008
- Indian Institute of Technology, Kanpur, January 2006.
- Indian Institute of Technology, New Delhi, January 2006.
- Chalmers University, Sweden, September 2004.
- Queens University, Canada, May 2004.
- McMaster University, Canada, February 2004.
- University of the West Indies, Barbados, December, 2002.
- Dartmouth College, October, 2002.
- University of the West Indies, Barbados, December, 2001.
- Wicker, S. B., "Evolutionary Game Theory and Self-Configuring Wireless Networks," UCLA, Los Angeles, CA, November 2, 2000.
- Wicker, S. B., "Optimization, Neural Networks, and Turbo Decoding," University of Ulm, Germany, July 23, 1999.
- Wicker, S. B., "Optimization, Neural Networks, and Turbo Decoding," Technical University of Munich, Germany, June 16, 1999.
- Wicker, S. B., "The Baum-Welch Algorithm and Turbo Decoding," Technical University of Denmark, Copenhagen, March 20, 1998.
- Wicker, S. B., "Maximum Likelihood Sequential Soft Decision Decoding for Block Codes," Jet Propulsion Laboratory/CalTech, Pasadena, California, December 30, 1997.
- Wicker, S. B., "Hard and Soft Decision Decoders for the FLEX Mobile Messaging Protocol," Motorola Paging Division, Fort Worth, Texas, November 24, 1997.
- Wicker, S. B., "Soft Decision and Turbo Error Control for Wireless

Multimedia Networks," Motorola Paging Division, Fort Worth, Texas, November 24, 1997.

- Wicker, S. B., "Turbo Codes, Bayesian Networks, and the Future of Telecommunications," SUNY Buffalo, Department of Electrical Engineering, May 23, 1997.
- Wicker, S. B., "Soft Decision Trellis Decoders for Block Codes: Thoughts on the State of the Art," Lancaster University, Lancaster, England , January 14, 1997.
- Wicker, S. B., "Introduction to the Cornell Wireless Multimedia Laboratory," Distinguished Seminar Series, Queen's University, November 13, 1996.
- Wicker, S. B., "Introduction to the Cornell Wireless Multimedia Laboratory," GTR Corporate Research and Development, Schenectady, New York, September 26, 1996.
- Wicker, S. B., "Enabling Technologies for Wireless Multimedia Systems," Strathclyde University, Glasgow, Scotland, August 15, 1996.
- Wicker, S. B., "Wireless Technologies and the Evolution Toward the Universal Mobile Telecommunication System," National Technical University of Athens, Athens, Greece, September 4, 1995.
- Wicker, S. B., "Wireless Technologies and the Evolution Toward the Universal Mobile Telecommunication System," University of Athens, Department of Telematics, Athens, Greece, September 5, 1995.
- Wicker, S. B., "Wireless Technologies and the Evolution Toward the Universal Mobile Telecommunication System," Telecommunications Systems Institute, Chania, Crete, September 7, 1995.
- Wicker, S. B., "Error Control Coding for Mobile Applications," Jet Propulsion Laboratory, Pasadena, California, October 18, 1994.
- Wicker, S. B., "Reed-Solomon Error Control Systems for Bidirectional Fading Channels", Lancaster University, Lancaster, England, June 21, 1994.
- Wicker, S. B., "Intelligent Systems for Error Control and Security", Defense Science and Technology Organization, Adelaide, South Australia, May 2, 1994.
- Wicker, S. B., "Reed-Solomon Error Control Systems for Bidirectional Fading Channels", Simon Fraser University, British Columbia, Canada, June 24, 1992.
- Wicker, S. B., "Reed-Solomon Error Control Systems for Bidirectional Fading Channels", University of British Columbia, Vancouver, British Columbia, Canada, June 23, 1992.
- Wicker, S. B., "Adaptive Error Control Using Convolutional and Trellis Codes", University of Victoria, Victoria, British Columbia, Canada, June 22, 1992.
- Wicker, S. B., "Reed-Solomon Error Control Systems for Bidirectional Fading Channels", University of Victoria, Victoria, British Columbia, Canada, June 19, 1992.
- Wicker, S. B., "Reed-Solomon Error Control Systems for Bidirectional Fading Channels", Institute of Communications Technology, German Aerospace Research Establishment, Oberpfaffenhofen, Germany, February 4 - 6, 1992.

- Wicker, S. B., "The Application of Classical Algebraic Geometry to Error Correcting Codes," Department of Mathematics, University of Puerto Rico, Rio Piedras, Puerto Rico, December 9 - 15, 1988.

Patents and Patent Applications

- Ober, C, O'Rourke, T, Spencer, M., Turner, J., Wicker, S., "Flexible Substrate Sensor System For Environmental And Infrastructure Monitoring", PCT WO 2008/140490, 20 November 2008, assigned to Cornell University.

- Fontaine, F. and Wicker, S., "Method and Apparatus for Turbo Decoding Block Codes", U.S. patent 7,243,288, June 10, 2007, assigned to Motorola.

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- Wang, X.-A. and Wicker, S. B., "The Analog Neural Net Viterbi Decoder," U.S. patent 5,548,684, August 20, 1996, assigned to Georgia Institute of Technology.

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Other Publications

- Alabbadi, M. and Wicker, S. B., "Integration of Error Correction, Encryption, and Signature Using Linear Error-Correcting Block Codes," *IEEE Information Theory Newsletter*, Volume 43, Number 4, p. 10, December 1993.

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- Harvey, B. A. and Wicker, S. B., "Adaptive Rate Convolutional Coding Using the Viterbi Decoder," *IEEE Information Theory Newsletter*, Volume 41, Number 3, p. 15, September 1991.

- Rice, M. D. and Wicker, S. B., "Adaptive Error Control over Slowly Varying Channels," *IEEE Information Theory Newsletter*, Volume 41, Number 2, p. 20, June 1991.

Funded Research Projects[1]

- TC: Privacy-Aware Design Strategies For Mobile Communications And Computing," National Science Foundation, $500,000, June 15, 2010 – June 14, 2013.

- "STC: Team for Research in Ubiquitous Secure Technology (TRUST)," National Science Foundation, $20,000,000, September 15, 2005 - September 15, 2015.

- "Nets-NOSS: NETS - NOSS: Ultra Low-Power, Self-Configuring, Wireless Sensor Networks," National Science Foundation, $2,000,000, September 15, 2004 - September 15, 2009.

- "ITR: Self-Configuring Sensor Networks for Disaster Mitigation and Recovery," National Science Foundation, $2,500,000, September 15, 2003 -- September 15, 2009.

- "SENSORS: The Reachback Channel in Wireless Sensor Networks," (PI: Sergio Sevetto), National Science Foundation. September 15, 2003 -- September 15, 2006.

- "The Ad Hoc Classroom: Integrating Emerging Wireless Communications and Networking Technologies into Mainstream Computer Science and Electrical Engineering Curricula," National Science Foundation-CRCD, (PI: Gun Sirer), $410,000, 2002 – 2005.

- "The Ad Hoc Classroom: Integrating Emerging Wireless Communications and Networking Technologies into Mainstream Computer Science and Electrical Engineering Curricula," Microsoft, (PI: Gun Sirer), $75,000, 2002 – 2005.

- "The Ad Hoc Classroom: Integrating Emerging Wireless Communications and Networking Technologies into Mainstream Computer Science and Electrical Engineering Curricula," Hewlett Packard, (PI: Gun Sirer), $20,000, 2002 – 2005.

- "Self-Configuring Wireless Sensor Networks," DARPA ITO, $900,000, June 1, 2000 - May 31, 2003.

- "Soft Decision Decoders for Wireless Systems," Motorola, $84,000, September 15, 1998 – September 15, 2000.

- "Sensor-Assisted Wireless Multimedia Systems," National Science Foundation Grant NCR-9725251, $862,465, September 15, 1997 - August 31, 2000 (with Terrence Fine and Joseph Halpern).

[1] Principal Investigator is Stephen Wicker unless otherwise noted.

- “Coded Diversity Combining and Channel Estimation for Wireless Data Communications,” National Science Foundation Grant NCR-9706592, $ 246,636, September 15, 1997 - August 31, 2000 (with Zygmunt Haas).

- AT&T/Lucent Technologies Foundation, Special Purpose Grant, $15,000, November 20, 1996.

- “Adaptive Code Division Multiple Access Systems,” National Science Foundation Grant Number Grant NCR-9505887, $ 236,855, September 15, 1995 - August 31, 1998

- “Data Transport on Cellular Telephone Systems,” Mobile Telecommunication Technologies International, $110,000, July 1, 1995 - June 30, 1996.

- “European Data Transfer Protocols,” Mobile Telecommunication Technologies International, $92,000, July 1, 1994 - June 30, 1995.

- "Soft Decision Decoding For Block Codes Using Artificial Neural Networks," National Science Foundation Grant Number NCR-9216686, $140,000, September 15, 1993 - March 14, 1996.

- “Adaptive Bandwidth-Efficient Coding for Nonstationary Channels,” National Science Foundation Grant NCR-9016276, $102,000, September 15, 1991 - March 14, 1994.

- “Cellular Mobile Telephony Laboratory,” Mitsubishi Consumer Electronics, $500,000 (Equipment), May 29, 1991.

- “Adaptive Coding on Nonstationary Communication Channels with Feedback,” National Science Foundation Grant NCR-9009877, $85,000, September 15, 1990 - September 14, 1993.

- “Young Faculty Grant,” General Electric, $10,000, July 15, 1989 - July 14, 1990.

- “Cellular Radio Diversity Simulation Study,” Bell South Mobility, Coprincipal Investigator: Gordon L. Stuber, $60,000, March 25, 1989 - June 25, 1989.

- “An Investigation of Message Handling in Post 2000 Era,” U. S. Army Signal Center, Fort Gordon, Coprincipal Investigator: Douglas W. Browning, $137,161, January 10, 1989 - December 31, 1989.

- “Cellular Radio Simulation and Coding Study,” Bell South Mobility, $35,000, December 15, 1988 - March 15, 1989.

- “Cellular Radio Spectrum Study,” Bell South Mobility, $30,000, September

25, 1988 - December 15, 1988.

- "The Algebraic Foundations of Digital Communication," AT&T Foundation, $25,000, July 7, 1988 - July 6, 1989.

- "Cellular Radio Spectrum Study," Bell South Mobility, $45,000, June 15, 1988 - September 15, 1988.

- "Cellular Radio Spectrum Study," Bell South Mobility, $40,000, March 15, 1988 - June 15, 1988.

- "Communication System Simulation Software Package," Space and Communications Group, Hughes Aircraft Company, $200,000 (software), February 1, 1988.

Service

Institute of Electrical and Electronic Engineers (IEEE)

- Elected to Board of Governors, IEEE Information Theory Society, 1996 – 1998, re-elected for 1999 - 2001.

- Information Theory Society representative to IEEE Committee on New Technology Directions

Defense Advanced Research Projects Agency (DARPA)

- Member, Information Science and Technology Study Group, 1999 – 2002.

Journals

- Editor, *ACM Transactions on Sensor Networks*, 2004 - present.

- Editor, Special Issue on Ad Hoc Networks, Volume 2, *IEEE Journal on Special Areas in Communications*, 2005.

- Editor, Special Issue on Sensor Networking, *IEEE Journal on Special Areas in Communications*, 2004.

- Editor, Special Issue on Ad Hoc Networks, *IEEE Journal on Special Areas in Communcations*, 2004.

- Editor, Special Issue on Energy-Aware Ad Hoc Wireless Networks, *IEEE Wireless Communications*, August 2002.

- Editor for Coding Theory and Techniques, *IEEE Transactions on Communications*, March, 1995 - March 2001.

- Reviewer for numerous journals, conferences, national and international funding agencies, and textbook publishers.

Conference Organization

- Chair, Technical Program Committee, Fifth International Symposium on Information Processing in Sensor Networks (IPSN 2006), Nashville, Tennessee.

- Member, Technical Program Committee, International Conference on Distributed Computing in Sensor Networks (DCOSS '06).

- Member, Technical Program Committee, Fourth International Symposium on Information Processing in Sensor Networks (IPSN 2005), Berkeley, California.

- Member, Technical Program Committee, Conference on Innovations and Commercial Applications of Distributed Sensor Networks, Bethesda, MD, October 18 –19, 2005.

- Member, Technical Program Committee, Second IEEE International Conference on Sensor and Ad Hoc Communications and Networks (SECON 2005).

- Member, Organizing Committee, First IEEE Conference on Sensor Networks: Applications, Protocols and Technology (SNAPT 2004).

- Member, Technical Program Committee, First Annual IEEE Communications Society Conference on Sensor and Ad Hoc Communications and Networks, Santa Clara CA, October 2004.

- Member, Technical Program Committee, Third International Symposium on Information Processing in Sensor Networks (IPSN '04), Berkeley, California, USA April 26-27, 2004

- Member, Organizing Committee, 7th International Symposium on Communication Theory and Applications, Ambleside, England, 2003

- Member, Technical Program Committee, First IEEE International Workshop on
Sensor Network Protocols and Applications, May 11, 2003, Anchorage, AK.

- Chair, IEEE Information Theory Society Symposia and Workshops Committee, 2000 - 2001.

- Organizing Committee, 6th International Symposium on Communication Theory and Applications, Ambleside, England, 2001

- Member, International Advisory Committee, 2000 International Symposium on Information Theory and its Applications, Honolulu, November 5 - 8, 2000.

- Technical Program Committee, 1999 IEEE Wireless Communications & Networking Conference (WCNC), New Orleans, LA, Sep. 22 - 27, 1999.

- Organizing Committee, 5th International Symposium on Communication Theory and Applications, Ambleside, England, 10-14 July, 1999

- Technical Program Committee, International Symposium on Information Theory and Applications, Mexico City, Mexico, October 14 - 16, 1998.

- Chaired "ARQ and Wireless Error Control" session at the 1998 International Symposium on Information Theory, Boston, MA, August 16-21, 1998.

- Organizing Committee, 4th International Symposium on Communication Theory and Applications, Ambleside, England, 11 - 15 July, 1997

- Technical Program Committee, International Symposium on Information Theory and Applications, Victoria, British Columbia, September 17-21, 1996.

- Organized and chaired "Gus Solomon Memorial Session" at IEEE Pacific Rim Conference on Communications, Computers, and Signal Processing, Victoria, British Columbia, August 20-22, 1997.

- Chaired "Mobile Communications" session at the International Symposium on Information Theory and Applications, Victoria, British Columbia, September 17-21, 1996.

- Chaired "Advanced Subsystems in Wireless Multimedia Networks" session at the Japan-Canada International Workshop on Multimedia Wireless Communications and Computing, Victoria, British Columbia, September 17, 1996.

- Technical Program Committee, IEEE Vehicular Technology Conference, Atlanta, Georgia, April 28 - May 1, 1996.

- Chaired "Communication Networks" session at the 3rd International Symposium on Communication Theory and Applications, Ambleside, England, 10 - 14 July, 1995.

- Chaired "Decoding Problems" session at Seventh Joint Swedish-Russian International Workshop on Information Theory, St. Petersburg, Russia, June 17 - 22, 1995.

- General Chairman, Wireless Security Workshop, Metz, France, February 10 - 11, 1995.

- U. S. Representative, International Advisory Board, IEEE International Symposium on Information Theory, Whistler, British Columbia, Canada, September 17 - 22, 1995.

- Chaired "Coding and Modulation" session at the 3rd UK/Australian International Symposium on DSP for Communication Systems, Warwick, UK, 12 - 14 December, 1994.

- Chaired "Error Control Techniques" session at 1990 IEEE International Conference on Communications, Atlanta, Georgia, April 16 - 19, 1990.

University Committees, Cornell University

- Chair, General Recruiting Committee, School of Electrical and Computer Engineering, (2009 – 2012)
- Member, University Local Advisory Committee (appointed by Faculty Senate) (2008 – 2011)
- Member, Faculty Advisory Board for Information Technology, (appointed by Faculty Senate) (2004 - 2007)
- Member, University Intellectual Property Advisory Committee, (appointed by VP for Research) (2003 - present)
- Chairman, College of Engineering Curriculum Governing Board (appointed) (2001 - 2002)
- Chairman, Electrical Engineering Curriculum and Standards Committee (elected) (2001 -2002)
- Chairman, Electrical Engineering Policy Committee (elected) (1998-2000)
- Chairman, Electrical Engineering PeopleSoft Lab Oversight Committee (1997-2003)
- Member, College of Engineering Dean Search Committee (2000-2002)
- Member, College of Engineering Teaching Award Committee (1999-2000)
- Member, Applied Mathematics Director Search Committee (1999)
- Member, Associate Dean Search Committee, 1998.
- Member, Electrical Engineering Policy Committee (elected) (1997-2000)
- Member, Digital Systems Search Committee (1997-1998)
- Member, College Faculty Advisory Committee for Associate Dean for Professional Development (1998)
- Chairman, Several Department and College Ad Hoc Tenure and Promotion Committees.

Institute Committees, Georgia Institute of Technology

- Institute Statutory Advisory Committee (elected) (1995 - 1997)
- Institute Public Relations Committee (elected) (1990 - 1992)
- ECE Graduate Curriculum Committee (1995 - 1997)

- ECE Undergraduate Curriculum Committee (1994 - 1995)
- ECE Computer Resources Committee (1988 - 1991)

Honors and Awards

- Fellow of the IEEE, 2011
- U.S. Air Force Scientific Advisory Board, 2010 - 2012
- Cornell University College of Engineering Teaching Award, 2009
- Cornell School of ECE Teaching Award, 2000
- Cornell University College of Engineering Teaching Award, 1998
- SAIC Best Paper Award, 1994, for "An Artificial Neural Net Viterbi Decoder" (with Xiao-an Wang)
- Senior Member, Institute of Electrical and Electronic Engineers. Elected January, 1993
- Visiting Fellow, British Columbia Advanced Systems Institute. Awarded January 1992.
- Sigma Xi, 1991 - present
- Tau Beta Pi, 1980 - present
- Eta Kappa Nu, 1980 - present
- Omicron Delta Kappa, 1980 – present